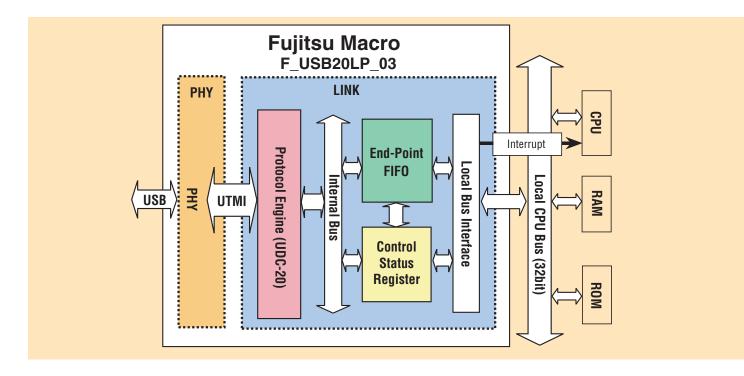


USB 2.0 Device Controller Macro



Features

- Full compliance with USB 2.0 Device Controller standard
- Integrated PHY macro for system cost reduction and space saving
- Supports high-speed (480Mbps) and full-speed (12Mbps)
- Flexible endpoint numbers and configurations

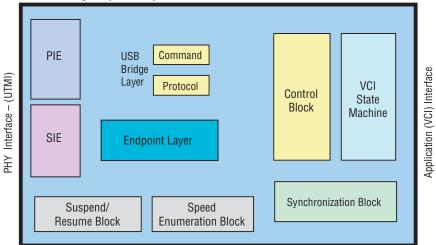
Description

- Link

- Protocol Engine (UDC-20) is a fully synthesizable soft core that supports high-speed (480 Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) signaling bit rates.
- UTMI (USB 2.0 Transceiver Macrocell Interface) enables connection with discrete PHY chip (ASSP) as well as integrated PHY.
- Protocol engine reduces CPU burden by processing basic USB 2.0 protocols in hardware.
- Endpoint numbers, configurations, and its FIFO densities are flexible. Following is one of the configuration examples.
 - 1) End Point 0 out control out 64Byte
 - 2) End Point 0 in control in 64Byte
 - 3) End Point 1 out Bulk out 512Byte (x2 Double buffer)
 - 4) End Point 2 in Bulk in 512Byte (x2 Double buffer)
 - 5) End Point 3 in Interrupt 64Byte

USB 2.0 Device Controller Macro

Protocol Engine (UDC-20) Internals



-PHY

- UTMI (USB 2.0 Transceiver Macrocell Interface) compliant
- PHY block consists of a 0.18um hard macro and a soft macro (Receiving Block).
- PHY block supports high-speed (480Mbps) and full-speed (12Mbps).
- Contains high-speed Analog Blocks and high-speed SERDES (serializer and de-serializer Logic) and provides a parallel interface to UDC-20 protocol Engine.
- 16bit/8bit parallel connection to Link

Applications

- PC Access Point to High-Speed Wireless Connectivity
- Digital Video and Still Cameras

- Digital Set Top Box and Cable Modems
- Printers and Scanners

Deliverables

Fujitsu's local application engineer will work with the customer closely to identify his specific IP requirements and select the most appropriate USB 2.0 device configuration that will best suit the customer's need. After the IP has been selected, the following database items can be provided to the customer:

- Encrypted Verilog RTL source code or Gate Level Netlist
- Synthesis Scripts (provided where applicable)
- User's Guide

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