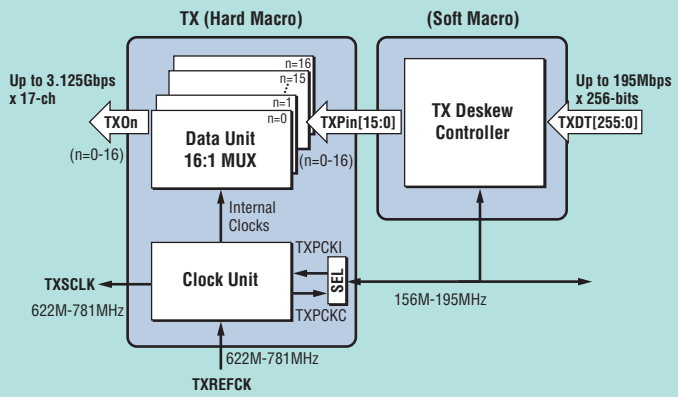
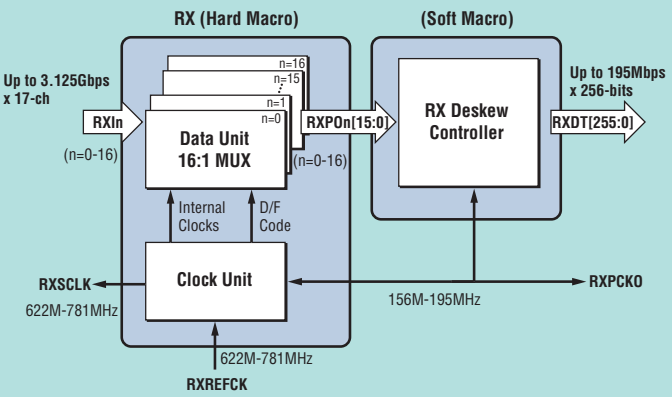
SERDES Framer Interface Level-5

OIF Compliant SFI-5 Source Synchronous Interface Macro

Transmitter Macro Structure



Receiver Macro Structure



Features

- 17-channel source synchronous transmitter and receiver arrays
- Differential CML interface for high-speed signals (SFI-5 compliant level)
- 1: 16 SERDES
- Synchronous data transfer with 622M-781MHz serial clock (quarter of data rate)
- Dynamic deskew function at receiver
- Integrated on-chip 50-ohm termination resistor for transmitter and receiver
- Programmable transmitter output current
- Integrated PRBS generator and comparator
- 1.2V and 2.5V supply, 0.11µm standard CMOS process

Benefits

- Industry standard OIF compliance
- Two power down operations
- Low power dissipation
- Boundry SCAN test support
- Available as library cell for ASIC designs

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Description

Fujitsu's SFI-5 compliant transceiver macro is a 17-channel physical I/O interface macro for ASICs that perform high bandwidth data communication while operating at low power consumption. The transceiver consists of a 17-channel transmitter unit, a 17-channel receiver unit and a bias unit. The transmitter and the receiver are compliant with OIF SFI-5 specification.

The macro is fabricated in Fujitsu's standard 0.11µm CMOS technology with supply voltage of 1.2V and 2.5V.

This macro can be used in a variety of applications:

- Long-haul optical transport equipment
- Metropolitan area network equipment
- Wavelength Division Multiplex (WDM) equipment
- Line Card applications for switches and routers
- Add Drop Multiplexers (ADM)

Deliverables

The Fujitsu value-added 3.125Gbps SFI-5 Compliant Transceiver Macro enables our customers to design a variety of complex system-on-a-chip ASIC designs for high-end networking applications, such as 40G.

A Fujitsu application engineer works with the customer to identify the customers' specific IP requirements. Fujitsu will provide the customer with the following information to support the 2.5-3.125Gbps Transceiver macro:

- Verilog Model
  - Front-end simulation
  - C model with Verilog wrapper
- Library Exchange Format (LEF)
  - Floor planning
- Design Compiler Model
  - Timing analysis
  - Place and Route

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