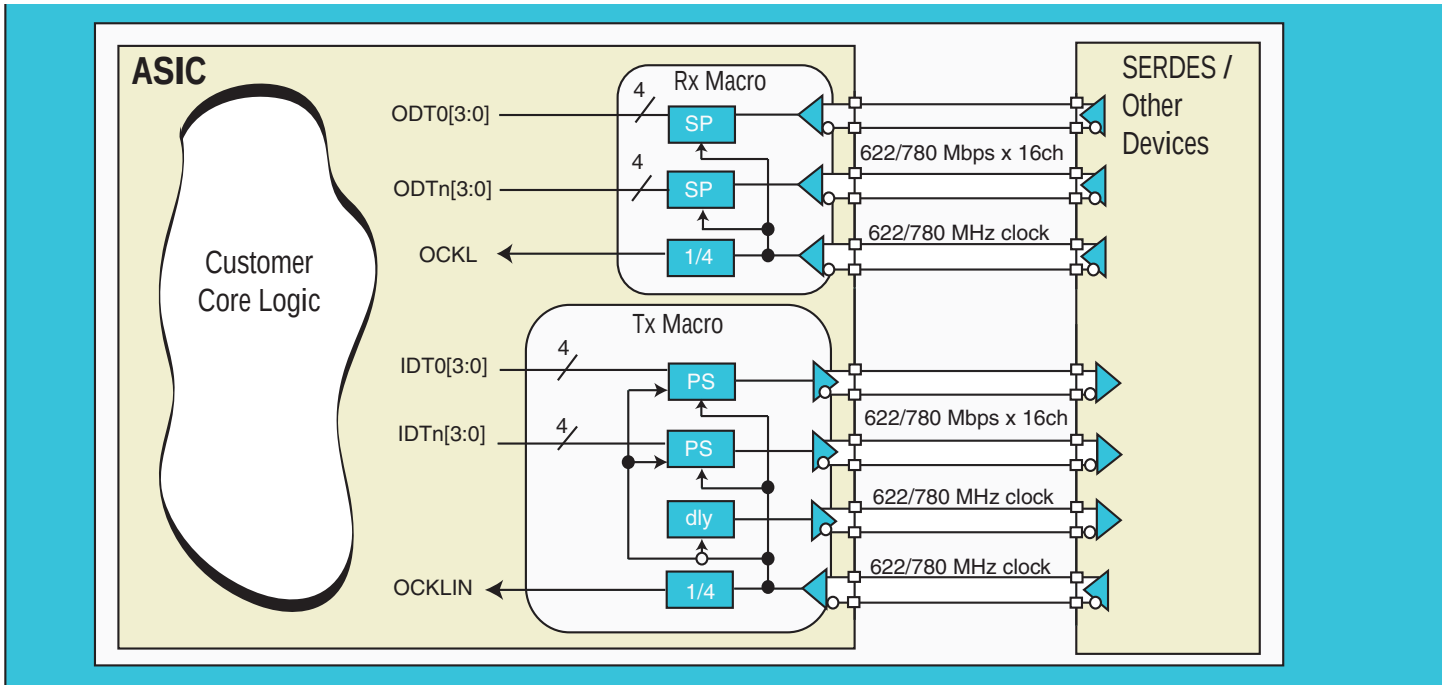
SERDES Framer Interface Level-4

OIF Compliant SFI-4 Source Synchronous Interface Macro



Features

- 16-channel OIF SFI4-1.0 standard compliant at 622/780Mbps per channel
- 10/12.5Gbps aggregate bandwidth rates in each direction
- Source Synchronous data transfer using 622/780 MHz clock
- Reciever macro is a source synchronous link of 16 data channels, each with 1:4 serial to parallel demultiplexer
- Trasmitter macro is a source synchronous link of 16 data channels, each with 4:1 parallel to serial multiplexer
- Differential LVDS interface on input and output pins
- Integrated on-chip termination resistors on transmitter and receiver
- Low power 0.92W for transmitter macro and 0.43W for the receiver macro with worst case conditions
- 1.8V and 3.3 V power supply
- 0.18 micron standard CMOS technology with triple well isolation

Benefits

- Hard macro for ASIC designs guarantees performance
- Supports 10/12.5 Gbps aggregate bandwidth for OC192, 10Gbps Ethernet and POS applications
- Easy interface to ASIC core logic due to internal path being demultiplexed 1:4 bits at 155/195Mbps rate

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Description

Fujitsu's SFI4-1.0 macro enables the interface of any two chips at an aggregate of 10 to 12.5Gbps in each direction. Sixteen 622/780 Mbps differential data lines (plus one clock) are provided in the transmit direction, and another sixteen (plus one clock) in the receive direction.

The framer ASIC transmits a 622/780MHz clock along with the data. The Receiver converts each of sixteen 622/780Mbps differential data lines to 4 parallel data bits at 155MHz for a total of 64. Each Transmitter channel (out of 16) converts 4 parallel data (out of 64 bits) at 155Mbps to one (out of 16) 622/780Mbps serial data.

For improved noise performance in an ASIC environment, the macro is fabricated in Fujitsu's advanced 0.18µm CMOS technology with triple well isolation.

Applications

The SFI4-1.0 interface macro can be used in a variety of applications:

- Gigabit and terabit routers
- Optical cross connect switches
- Network management systems
- DWDM and SDH transmission systems

Deliverables

The Fujitsu value-added SFI4-1.0 interface macro enables our customers to design a variety of complex system-on-a-chip ASIC designs for high-end networking applications. A Fujitsu application engineer works with the customer to identify the customers' specific IP requirements. Fujitsu will provide the customer with the following information to support the SFI4-1.0 macro:

- Verilog Model
  - Front-end simulation
- Design Compiler Model
  - Timing analysis
  - Place and Route
- Library Exchange Format (LEF)
  - Floorplanning

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