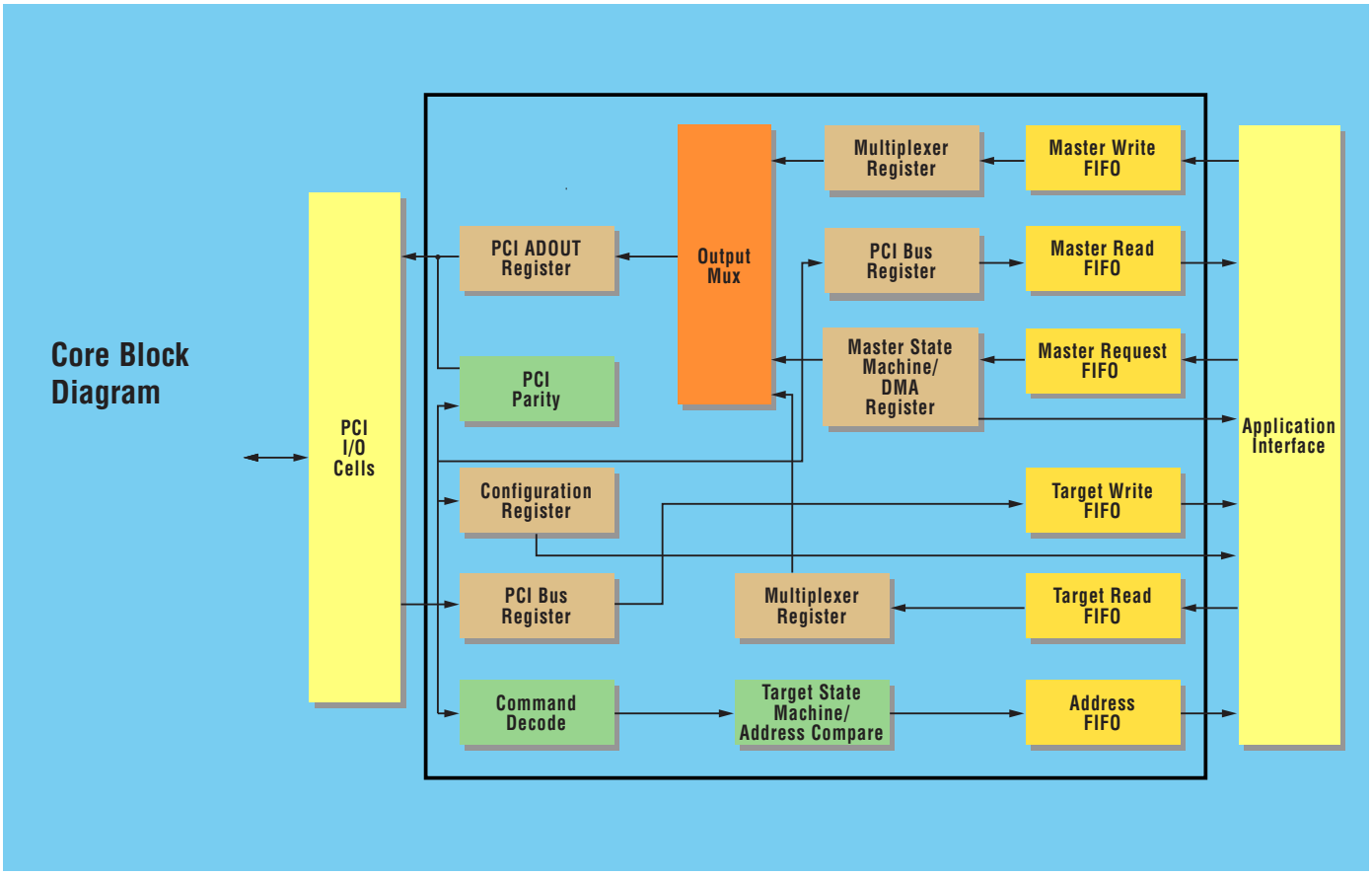
PCI Peripheral Core

FUJITSU



Features

- PCI V2.1 compliant
- 32-bit or 64-bit PCI Bus
- 32-bit or 64-bit Application Datapath
- 33 MHz and 66 MHz Speed Options
- Fast back-to-back Master Cycles Support
- Full Bandwidth Burst Support
- Read-only PCI Configuration Register can be optionally downloaded from an EEPROM at system start-up
- Memory Write and Invalidate Support
- Dual Address Cycles Support

Benefits

- Soft core that can be implemented in any technology
- Rigorous testing performed to ensure PCI compliance and functional correctness for a wide range of operations
- Synchronous or asynchronous application interfaces
- Internal scan and JTAG boundary scan can be inserted by customer before netlist handoff or by Fujitsu after handoff

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Description

The PCI Synthesizable Core is a part of the Fujitsu IPWare™ Library. The Fujitsu PCI Cores are RTL synthesizable modules that provide an interface between an application and the PCI bus. All PCI protocol and timing requirements are handled by the core, which is controlled through a simple application interface.

The Fujitsu PCI Cores are available in 32-bit or 64-bit bus paths on either the PCI bus or the application interface. The FIFO can be configured to different depths. Also, Fujitsu can provide these cores without any FIFOs.

The Fujitsu PCI Core family is architected for 33 MHz and 66 MHz performance, and verified through a combination of logic synthesis, floorplanning, place and route, and post layout timing verification with deep-submicron libraries.

The PCI Cores offer synchronous or asynchronous application interfaces. Asynchronous PCI Cores synchronize control and data signals between the PCI clock and an application clock, which may operate at a different frequency. The synchronous PCI Cores assume that all signals to and from the application are synchronized to the PCI clock.

The read-only register within the PCI configuration space can be optionally downloaded from an EEPROM at system startup. Information such as vendor ID, which is typically hard-coded into the chip incorporating the PCI core, can be loaded at system start. This allows the same chip to be used in more than one system.

Deliverables

The Fujitsu family of application-optimized synthesizable PCI cores has become the de facto standard for designers who need high PCI performance, off-the-shelf availability, and fast incorporation into ASIC designs.

Fujitsu's application engineer works with customers and helps them select process technology that will suit the customer's specific need. After the technology is selected, the following can be supplied to the customer:

- Encrypted RTL source codes written in Verilog and representing the entire hierarchical PCI core design
- A hierarchical gate level netlist of the PCI core

FUJITSU MICROELECTRONICS AMERICA, INC.

Corporate Headquarters
1250 East Arques Avenue, Sunnyvale, California 94088-3470
Tel: (800) 866-8608 Fax: (408) 737-5999
E-mail: inquiry@fma.fujitsu.com Web Site: http://www.fma.fujitsu.com

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