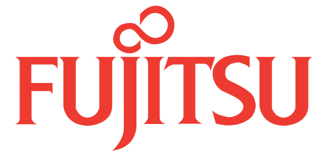
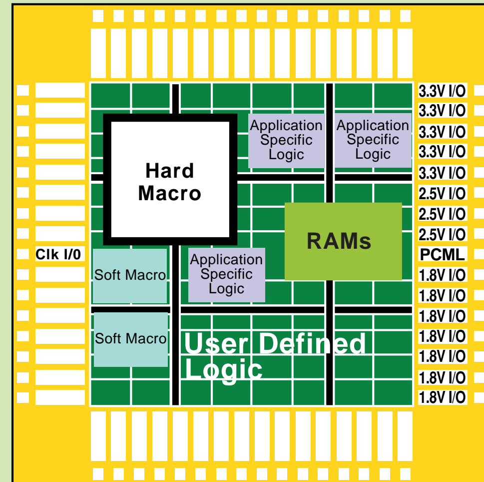
CE81 Series Embedded Array



0.18µm CMOS Technology

Features

- 0.13µm effective channel length
- 3 to 5 layers of metal interconnects
- Very high-density: 86K raw gates/mm^2
- Up to 23 million gates
- Core power supply voltage: 1.8V to 1.1V
- 8 nW/gate/MHz power dissipation at 1.1V
- 12 ps gate delay at 1.8V and 1 fan-out
- Junction temperature range: –40 to +125 °C
- I/Os: 3.3V, 2.5V, 1.8V, 5V tolerant
- High-density diffused RAMs and ROMs
- High-speed mixed-signal macros
- Analog PLLs
- Wide selection of advanced packaging options
- Proven design methodology and tool support



Description

Fujitsu's CE81 is a series of high performance, 0.18µm (0.13µm L_{eff}) CMOS embedded arrays that include full support of diffused high-speed RAMs, ROMs, analog, mixed-signal macros, and a variety of embedded functions.

The CE81 series offers density and performance similar to those of standard-cell implementation, yet has the time-to-market advantage of gate arrays. The CE81 series devices include 44µm, 66µm, or 70µm pad pitch for a cost-effective solution for both pad-limited and core-limited designs. The inline pads are available in both 70µm and 44µm pad pitch. The 70µm pads are wire bonded, whereas the 44µm pads are used with TAB. The 66µm wire-bond stagger pads can be used for optimizing the die area of pad-limited designs.

The CE81 chip cores can operate at 1.8V to 1.1V. The I/Os, operating at 1.8V, 2.5V, or 3.3V, can conveniently interface with various types of devices. The CE81, which features very low power and high density, is well suited for hand-held computing, graphics, communication and consumer electronics applications.

A-Series with 44µm Inline Pad Pitch and TAB

Frame	Total Gates	Total Pads
A4	1,032K	304
A5	1,370K	352
A6	1,930K	420
A7	2,930K	520
A8	4,137K	620
A9	5,552K	720
AA	7,039K	812
AB	8,394K	888
AC	9,787K	960
AD	11,300K	1,032
AE	14,045K	1,152

I-Series with 70µm Inline Pad Pitch

Frame	Total Gates	Total Pads
I1	527K	144
I2	791K	176
I3	1,110K	208
I4	1,483K	240
I5	1,689K	256
I6	2,385K	304
I7	3,207K	352
I8	4,150K	400
I9	5,791K	472
IA	7,249K	528

CE81 Series Embedded Array

S-Series with 66µm Stagger Pad Pitch		
Frame	Total Gates	Total Pads
SA	7,852K	585
SB	9,203K	632
SC	10,658K	680
SD	12,235K	728
SE	15,085K	808
SF	19,580K	920
SG	23,532K	1,008

Mixed-Signal Macros

- A/D Converters
  - 8-bit: 50 MS/s high-speed 3.3V
  - 8-bit: 25 MS/s high-speed 3.3V
  - 8-bit: 1 MS/s 3.3V
- D/A Converters
  - 10-bit: 30 MS/s 3.3V
  - 8-bit: 50 MS/s 3.3V
  - 8-bit: 1 MS/s 3.3V

Multiplier Compiler

- Multiplicand (m): $4 \leq m \leq 32$
- Multiplier (n): $4 \leq n \leq 32$ (even numbers only)

Memory Macros

- SRAM Compiler: single and dual port (1 RW/1R), up to 72K bits per block
- High-speed SRAMS, up to 144K bits per block
- High-density SRAMS (1 RW), 512K~ 1.1M bits (under development)
- Register files: 2R/2W
- ROM Compiler: up to 512K bits per block

Phase-Locked Loops

- Analog: up to 800 MHz

I/Os

- 1.8V, 2.5V, and 3.3V CMOS (2.5V is under development)
- Slew-rate controlled
- Capable of driving large loads: 2, 4, 8, and 12 mA sinking current
- Transceivers under development: P-CML, LVDS, PCI, SSTL, and GTL+
- AGP 2X and 4X
- 2.5 Gbps with clock recovery and Serdes (under development)
- To be developed: 5V tolerant buffers

SOC IP Cores

- ARC 32-bit RISC
- 10/100 MAC
- 64/256 QAM
- MPEG2 Decoder/Demultiplexer
- 8VSB TV Demodulator
- AC3 Dolby Voice Decoder
- JPEG Encoder and Decoder
- PCI – 33/66 MHz, 32/64-bit cores
- USB Host Controller/Device
- I^2C
- IDE (ATA3) Host Controller
- Smart Card I/F
- IRDA I/R Interface
- To be developed:
  - ARM 7TDMI Hard Macro
  - Oak DSP Hard Macro
  - More IPs are being added

ASIC Design Kit and EDA Support	
Verilog Logic Simulators from Cadence, Synopsys, and Mentor	Verilog-XL, NC-Verilog, VCS, Model-sim (Verilog)
VHDL/VITAL Logic Simulators from Synopsys, Cadence, and Mentor	VSS, Model-sim (VHDL), V-System, Leapfrog
Synthesis, DFT, and STA tools from Synopsys	Design Compiler, Test Compiler, and PrimeTime
Other EDA Tools	Chrysalis Design Verifyer and Sente Watt Watcher

PACKAGE AVAILABILITY No. of Pins	Frame Size
Thin QFP Package (0.5 mm pin pitch)	
100	I1, I2
120	I1, I2
Low-profile QFP Package (0.5 mm pin pitch)	
144	I1, I2
176	I2, I3
208	I4, I5
Heat-spread QFP Package (0.5 mm pin pitch)	
208	I3, I4, I5
240	I4, I5, I6, I7
304	I7, I8, I9, IA, SB, SC, SD, SE, SF, SG
Heat-spread QFP Package (0.4 mm pin pitch)	
256	I6, I7, I8, I9
TAB Ball Grid Array (0.8 mm ball pitch)	
304	A4, A5
352	A5, A6
TAB Ball Grid Array (1.0 mm ball pitch)	
480	A6, A7
560	A7, A8
660	A8, A9
720	A9, AA, AB, AC, AD, AE
Enhanced Ball Grid Array (1.27 mm ball pitch)	
576	SA, SB
672	SC, SD
Fine-pitch Ball Grid Array (0.8 mm ball pitch)	
112	I1, I2
144	I1, I2
168	I3
176	I3
192	I4, I5
224	I5, I6
272	I6, I7, I8
320	I8
Fine-pitch Ball Grid Array (0.75 mm ball pitch)	
288	I6, I7, I8, I9, IA
Fine-pitch Ball Grid Array (0.5 mm ball pitch)	
112	I1, I2, I3
176	I2, I3, I4, I5, I6
240	I6, I7, I8
304	I8, I9
368	IA

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