MB86R12 Application Note

DDR2 Interface

PCB Design Guideline

March, 2012
The 1.0 edition

FUJITSU

Preface

This guideline describes PCB design restrictions related to MB86R12 DDR2 interface signal wiring.

Revision History

Date	Ver.	Contents
2012/3/27	1.0	Newly issued

Contents

1. Floor plan

Figure 1-1 shows the reference example of the floor plan of MB86R12 and connected DDR2 SDRAM devices.

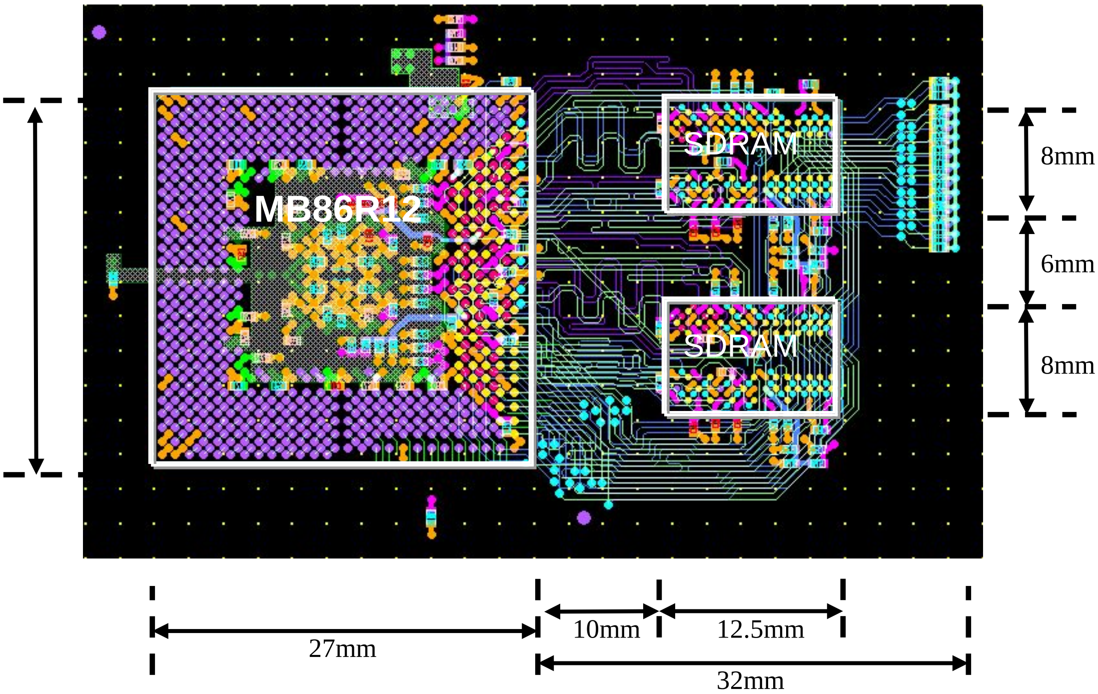


Figure 1-1 Reference example of the floor plan of MB86R12 and DDR2 SDRAM devices

2. PCB laminating

This chapter shows the recommended laminating conditions of the PCB.

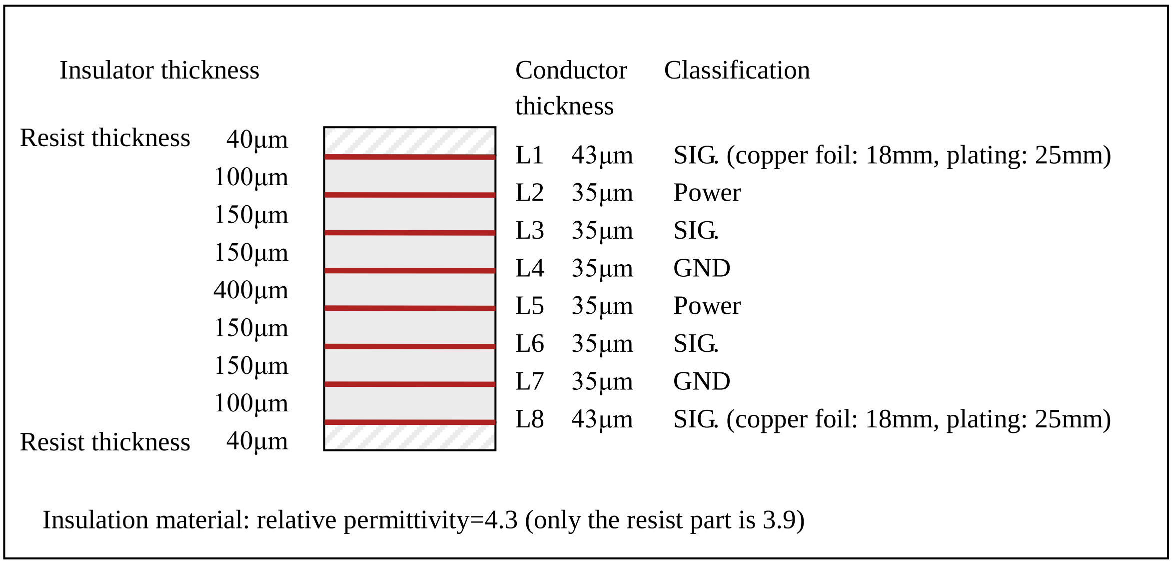


Figure 2-1 PCB laminating

Specified condition of wiring layer

- L1 and L8 are used as wiring and pull-out wiring layer of CLK.
- L3 and L6 are used as wiring layer of DQS, DQ, and CMD/ADD.
- L2 and L5 are used as power layer.
- L4 and L7 are used as GND layer.

3. DDR2_SDRAM specifications

This chapter shows DDR2_SDRAM that can be used for the DDR2 interface with MB86R12.
If an alternative device fulfills the same requirements, it can also used.
Please note however, that if you use an alternative device, there may be differences concerning I/O quality which may require your attention. However, all I/O characteristics should be checked as could differ.
Even if you use the device(s) listed below, you must refer to the specifications provided by the DRAM manufacturer for the confirmation of details (e.g. operating temperature conditions etc.).

Table 3-1 Recommended DDR2_SDRAM

Manufacturer	Product name	IBIS model name	Driver strength	Remarks
Micron Technology, Inc.	MT47H128M16RT-25E (2Gb 800Mbps)	u69a_at.ibs	FULL	It has already been verified by the transmission line analysis.

4. Signal design restrictions (DDR2 interface part)

This chapter describes the signal wiring design restrictions for the DDR2 interface part.

4.1. Definition of signal line group

In order to make the requirements for wiring configurations described further on in this document easier to understand, the DDR2 interface signals are classified into the groups listed below.

Table 4-1 DDR2 interface signal grouping

Wiring preferential order	Group name	Pin name of MB86R12
1	MCK_Group	MCK, MXCK
2	MDQS0_Group	MDQS0, MXDQS0
	MDQS1_Group	MDQS1, MXDQS1
	MDQS2_Group	MDQS2, MXDQS2
	MDQS3_Group	MDQS3, MXDQS3
3	MDQ0_Group	MDQ0~MDQ7, MDM0
	MDQ1_Group	MDQ8~MDQ15, MDM1
	MDQ2_Group	MDQ16~MDQ23, MDM2
	MDQ3_Group	MDQ24~MDQ31, MDM3
4	MCNTL_Group	MCKE, MXCS, MODT
5	MCMD_Group	MA0~MA14, MBA0~MBA2, MXCAS, MXRAS, MXWE

4.2. General wiring restrictions

This section describes the general wiring restrictions.

- It is recommended that signal wiring be designed to have the following characteristic impedance.
  Single impedance: 50Ω±10%
  Differential impedance: 100Ω±10%
- Signal wiring on power layer and GND layer should be sufficient width to guarantee the flow of return current. (Signal line should be wired on the same power group or GND group. It must not cross over other power and GND groups.)
- Please use parallel wiring for the positive and negative signals of the differential MCK_Group and MDQSx_Group signals. In addition, also take care that the position and number of layer vias is the same.
- The following groups must wire the same layer respectively, and the number of layer transfer vias must become the same, too.
  MDQS0_Group and MDQ0_Group
  MDQS1_Group and MDQ1_Group
  MDQS2_Group and MDQ2_Group
  MDQS3_Group and MDQ3_Group
  There are no restrictions to the number of layer transfer vias for other signals, but use a minimum possible.
- When using meander wiring layouts for signal delay, crosstalk may occur and the delay value reduced, therefore having wider spacing between wirings is recommended. The recommended wire spacing is about five times the wiring width.

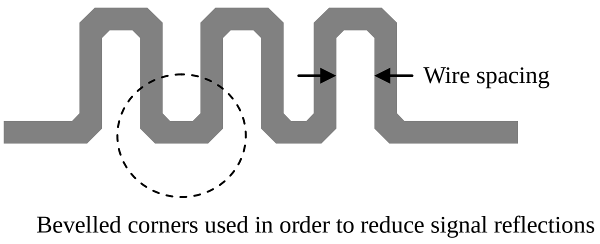


Figure 4-1 Meander wiring

The recommended conditions and the simulation waveform which are described further on in this document are valid under the above conditions.
If your design greatly differs from the above conditions, then please run a simulation on your wiring.

4.3. Resistance

- Resistors described in this guideline should be generally selected from the E12 series.
  E12 series: 10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82

- The following resistance tolerance values should be used (according to the resistance type):
  Terminal resistance: under ±5%
  Divider resistance for VREF: under ±1%

4.4. Terminal resistance/Damping resistance/Wire length

Table 4-2 shows the recommended resistance value and wire length for each group.
The wiring topology diagram relevant to this section is shown in "4.7. Wiring topology".

Table 4-2 Resistance value and wire length list

No.	Group name	External terminal resistance value (Rt)	Damping resistance value (Rd)	Wire length from MB86R12 output to SDRAM input	Internal group approved wire length variation
1	MCK_Group	39Ω × 2 0.1μF capacitor × 1 (Refer to "4.7.1.")	N/A	Refer to "4.7.1."	Meet the conditions of "4.7.1."
2	MDQSx_Group	N/A	N/A	Refer to "4.7.2."	Meet the conditions of "4.7.2."
3	MDQx_Group	N/A	N/A	Refer to "4.7.3."	Meet the conditions of "4.7.3."
4	MCNTL_Group	33Ω	N/A	Refer to "4.7.4."	Meet the conditions of "4.7.4."
5	MCMD_Group	33Ω	N/A	Refer to "4.7.4."	Meet the conditions of "4.7.4."

4.5. Wiring gap/Crosstalk

Please keep to the wiring configurations shown below in order to avoid malfunctions and deteriorated signal integrity due to crosstalk.

(1) The recommended gap for wiring within MDQx_Group and MCMD_Group groups should be over 300µm.

Figure 4-2 Gap for wiring within MDQx_Group and MCMD_Group

(2) The gap for wiring with other groups should be over 300µm.

Figure 4-3 Gap for wiring of other signal groups

(3) Differential wiring signals of MCK_Group and MDQSx_Group should use a wiring gap of over 500µm to other signals.
If it is difficult to guarantee a gap above 500µm, separate the wire from other signals using a GND area. However, please take the consequent decrease of the wiring impedance into consideration.

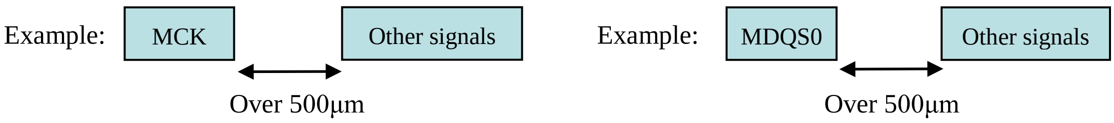


Figure 4-4 Gap for wiring between signal in MCK_Group/MDQSx_Group and other signals

4.6. ZQ/ODT setting

Table 4-3 shows the ZQ setting conditions.

Table 4-3 ZQ setting conditions

Group name	Output impedance of MB86R12 I/O (RON)	ZQ setting of MB86R12
MCK_Group	40Ω	Perform the ZQ calibration, and set it automatically.
MDQSx_Group	50Ω	
MDQx_Group	50Ω	
MCNTL_Group	40Ω	
MCMD_Group	40Ω	

Table 4-4 shows the recommended ODT setting conditions for MDQSx_Group and MDQx_Group signals.

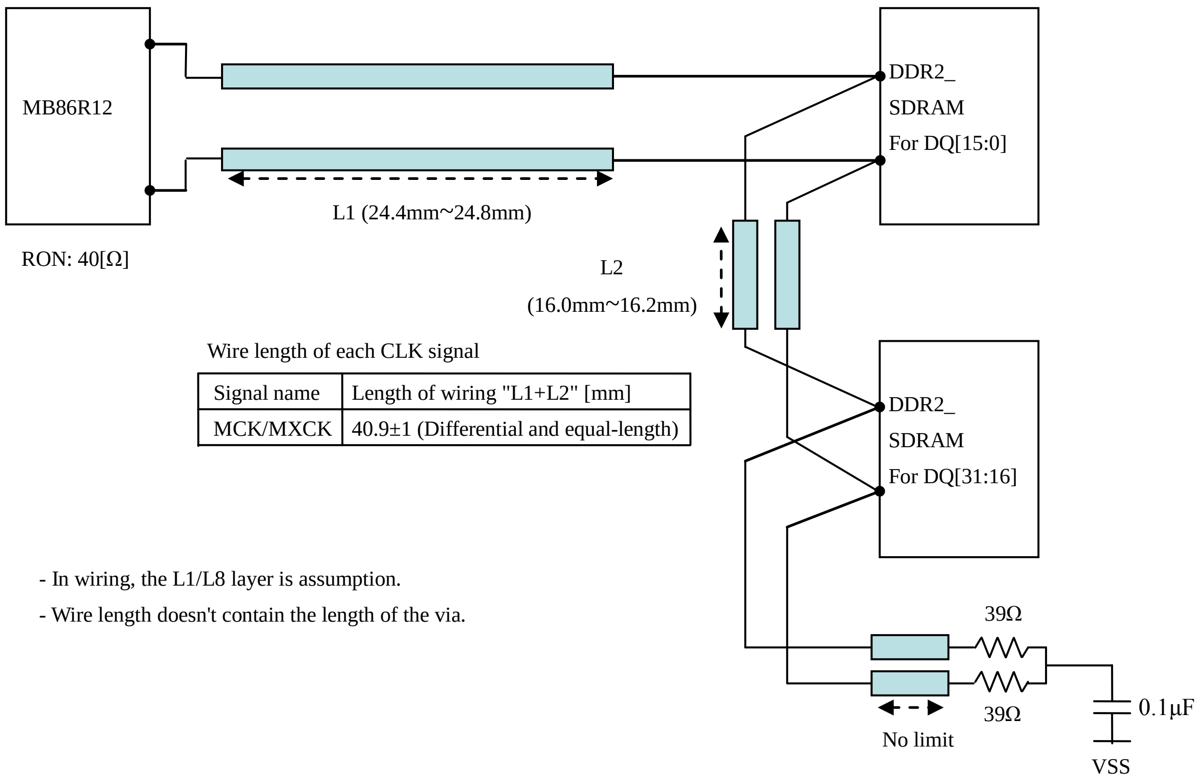
Table 4-4 ODT setting conditions

Operating condition	MB86R12	DDR2_SDRAM
Write to DDR2_SDRAM	Off	75Ω
Read from DDR2_SDRAM	50Ω	Off

4.7. Wiring topology

This section illustrates the recommended wiring topology of each group.

4.7.1. Wiring topology diagram of MCK_Group

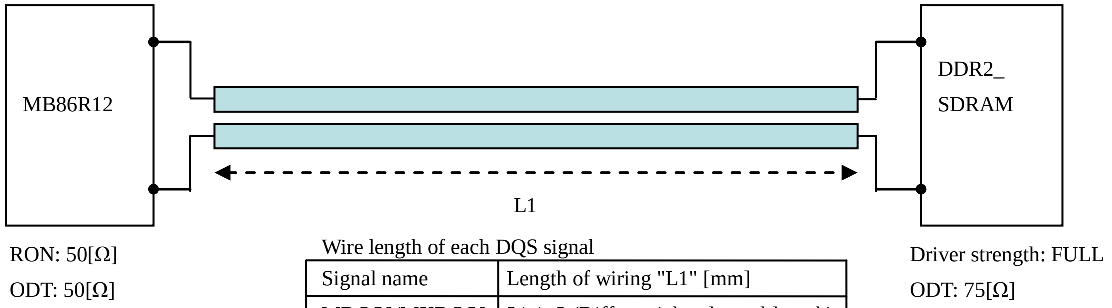


Wire length of each CLK signal

Signal name	Length of wiring "L1+L2" [mm]
MCK/MXCK	40.9±1 (Differential and equal-length)

Figure 4-5 Wiring topology diagram of MCK_Group

4.7.2. Wiring topology diagram of MDQSx_Group



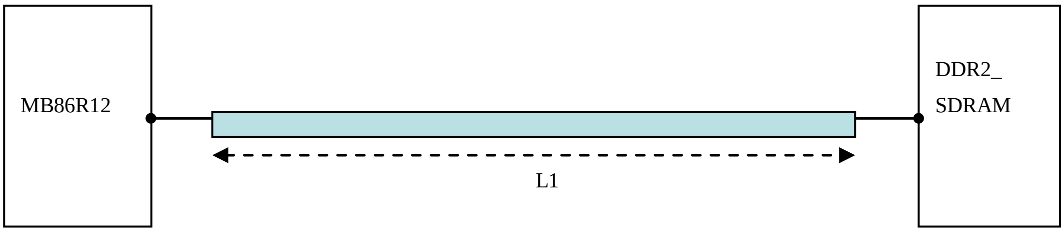
Wire length of each DQS signal

Signal name	Length of wiring "L1" [mm]
MDQS0/MXDQS0	31.1±3 (Differential and equal-length)
MDQS1/MXDQS1	31.7±3 (Differential and equal-length)
MDQS2/MXDQS2	30.7±3 (Differential and equal-length)
MDQS3/MXDQS3	28.8±3 (Differential and equal-length)

- In wiring, the L3/L6 layer is assumption.
- Wire length doesn't contain the length of the via.

Figure 4-6 Wiring topology diagram of MDQSx_Group

4.7.3. Wiring topology diagram of MDQx_Group



RON: 50[Ω]
ODT: 50[Ω]

Driver strength: FULL
ODT: 75[Ω]

- In wiring, the L3/L6 layer is assumption.
- Wire length doesn't contain the length of the via.

Wire length of each DQ signal

Signal name	Length of wiring "L1" [mm]	Signal name	Length of wiring "L1" [mm]
MDM0	Wire length of MDQS0_Group (Average value): +3.5±2	MDM2	Wire length of MDQS2_Group (Average value): +5.1±2
MDQ0	Wire length of MDQS0_Group (Average value): +2.9±2	MDQ16	Wire length of MDQS2_Group (Average value): +2.0±2
MDQ1	Wire length of MDQS0_Group (Average value): +2.8±2	MDQ17	Wire length of MDQS2_Group (Average value): +0.9±2
MDQ2	Wire length of MDQS0_Group (Average value): +2.2±2	MDQ18	Wire length of MDQS2_Group (Average value): +4.5±2
MDQ3	Wire length of MDQS0_Group (Average value): +1.1±2	MDQ19	Wire length of MDQS2_Group (Average value): +2.7±2
MDQ4	Wire length of MDQS0_Group (Average value): +2.7±2	MDQ20	Wire length of MDQS2_Group (Average value): +4.1±2
MDQ5	Wire length of MDQS0_Group (Average value): +5.0±2	MDQ21	Wire length of MDQS2_Group (Average value): +4.8±2
MDQ6	Wire length of MDQS0_Group (Average value): +3.6±2	MDQ22	Wire length of MDQS2_Group (Average value): +3.3±2
MDQ7	Wire length of MDQS0_Group (Average value): +1.1±2	MDQ23	Wire length of MDQS2_Group (Average value): +2.5±2
MDM1	Wire length of MDQS1_Group (Average value): +2.5±2	MDM3	Wire length of MDQS3_Group (Average value):） +4.7±2
MDQ8	Wire length of MDQS1_Group (Average value): +4.4±2	MDQ24	Wire length of MDQS3_Group (Average value): +3.2±2
MDQ9	Wire length of MDQS1_Group (Average value): +3.1±2	MDQ25	Wire length of MDQS3_Group (Average value): +1.3±2
MDQ10	Wire length of MDQS1_Group (Average value): +1.4±2	MDQ26	Wire length of MDQS3_Group (Average value): +5.9±2
MDQ11	Wire length of MDQS1_Group (Average value): +3.3±2	MDQ27	Wire length of MDQS3_Group (Average value): +3.4±2
MDQ12	Wire length of MDQS1_Group (Average value): +2.2±2	MDQ28	Wire length of MDQS3_Group (Average value): +6.6±2
MDQ13	Wire length of MDQS1_Group (Average value): +2.9±2	MDQ29	Wire length of MDQS3_Group (Average value): +3.9±2
MDQ14	Wire length of MDQS1_Group (Average value): +4.2±2	MDQ30	Wire length of MDQS3_Group (Average value): +5.0±2
MDQ15	Wire length of MDQS1_Group (Average value): +2.1±2	MDQ31	Wire length of MDQS3_Group (Average value): +6.4±2

Note 1) The DQ signal can be shuffled in byte.

Figure 4-7 Wiring topology diagram of MDQx_Group

4.7.4. Wiring topology diagram of MCNTL_Group/MCMD_Group

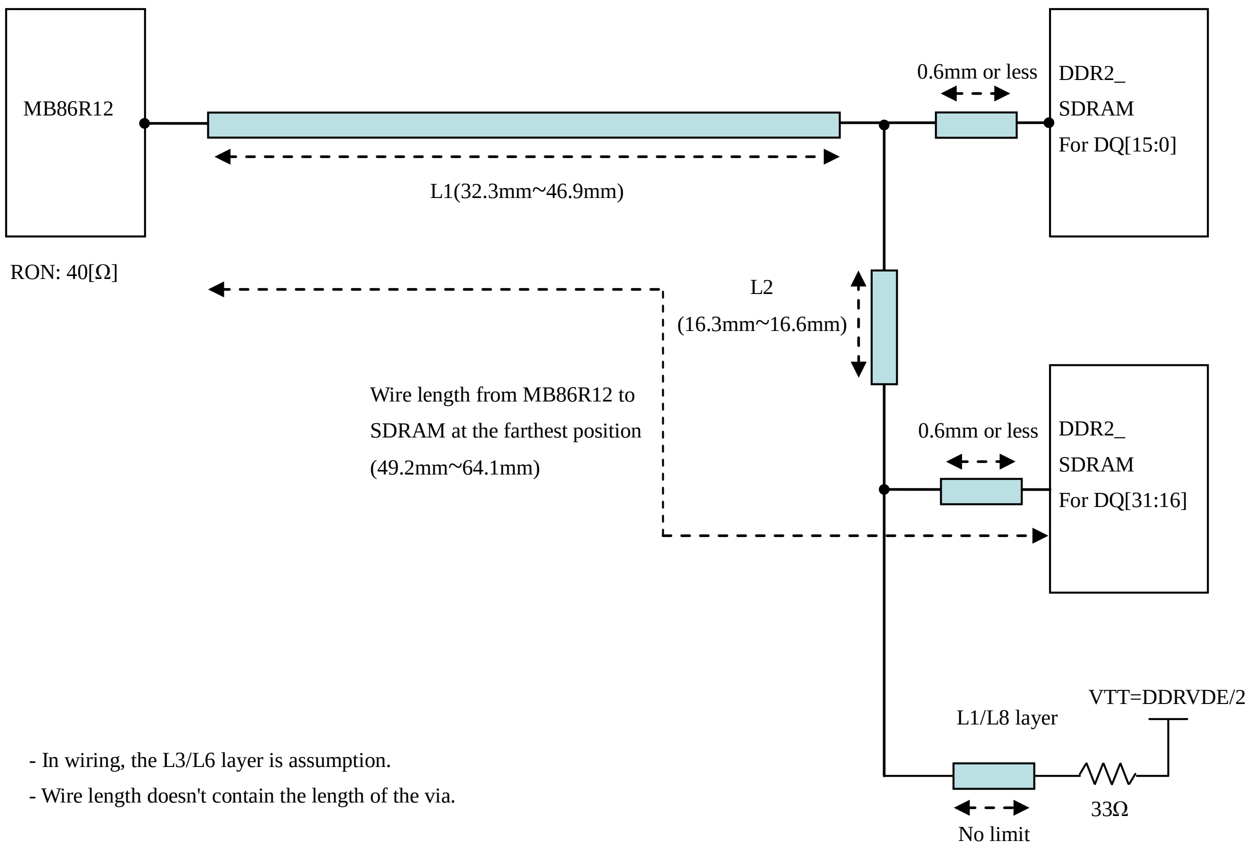


Figure 4-8 Wiring topology diagram of MCNTL_Group/MCMD_Group

5. Power system design restrictions

This chapter describes the power system design restrictions for the DDR2 interface part of MB86R12.

5.1. Number and capacity of bypass capacitor

Table 5-1 shows recommended number of bypass capacitors for the high frequency noise removal for which mounting is necessary directly under MB86R12.

Table 5-1 Recommended number of bypass capacitors

Pin name of MB86R12	Power supply voltage	Recommended number of bypass capacitors	Remarks
		0.1µF	
DDRVDE	1.8V	18	For DDR2 interface
VSS	0V	-	

- If capacity is a value close to 0.1µF (0.22µF etc. for instance), the bypass capacitor can be used.
- Place the 0.1µF capacitor as close as possible to the power/GND pins of MB86R12 (refer to "5.2. Pull-out wiring condition".
- For the 0.1µF capacitor, we recommend the use of ceramic capacitors of under size 1005 (1.0mm × 0.5mm).
  In addition, use low ESL (Equivalent Series Inductance) value components where possible in order to decrease noise.
- Mount a high-capacity capacitor for the low frequency if needed. One 100µF is recommended to be used for the current variation of 1A only as a guide.
- Verify your board design by simulations and measurements if you can not mount capacitors of the above number.

5.2. Pull-out wiring condition

This section shows the example of mounting the bypass capacitor for the high frequency noise removal. Be sure to meet the following pull-out wiring conditions to reduce the inductance value by wiring and to reduce the noise. If it doesn't meet these conditions, widen the wire width as much as possible, and shorten the wire length.

Note 1) There is no problem even if the Chip on Via method without the pull-out wiring is used.

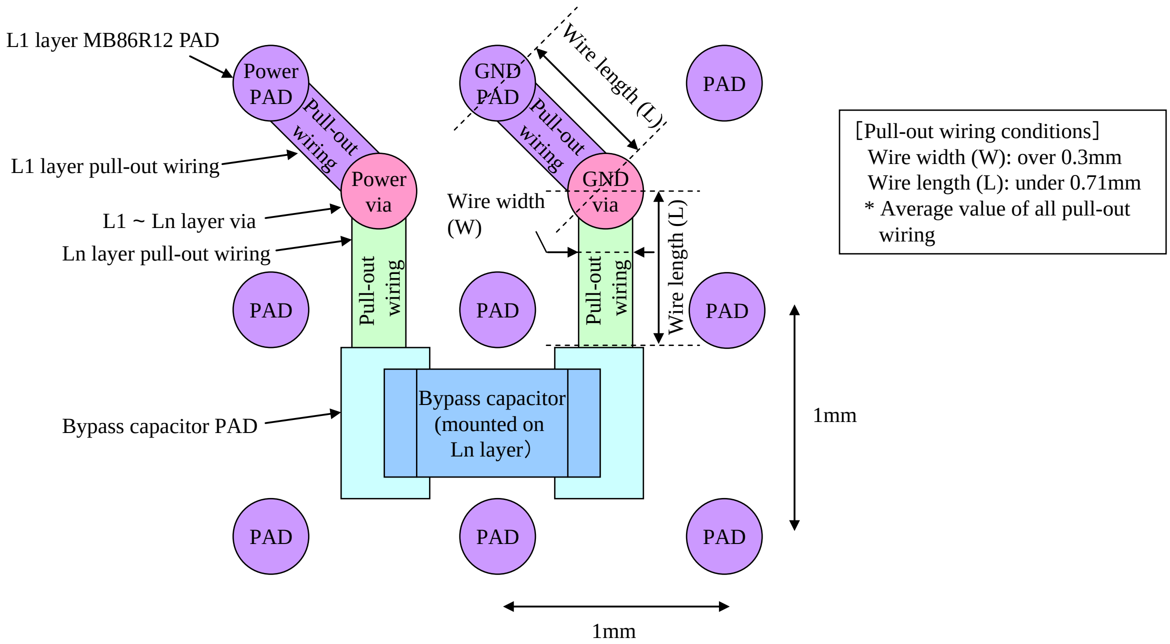


Figure 5-1 Example of mounting a bypass capacitor