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Using More than Two Displays with the Fujitsu Graphics SoC MB86R01 "Jade" Application Note

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Introduction

In order to use more than two displays with the Fujitsu Graphics SoC MB86R01 "Jade," both display controllers must be enabled. At least one of the display controllers will have to drive two displays in Multiplex Dual Display Mode. External demultiplexing logic should be used to separate the RGB content for each display. If four displays are needed, the other display controller can also be used in the Multiplex Dual Display Mode. Otherwise a single display can be connected directly to the second display controller. Figure 1 illustrates how three displays can be connected to the MB86R01 "Jade" Graphics SoC. The subsequent discussion is based on the assumption that MB86R01 "Jade" will be used in this configuration.

Display 0 and 1 must have identical display timing and resolution. Display 2 can have different display timing and resolution.

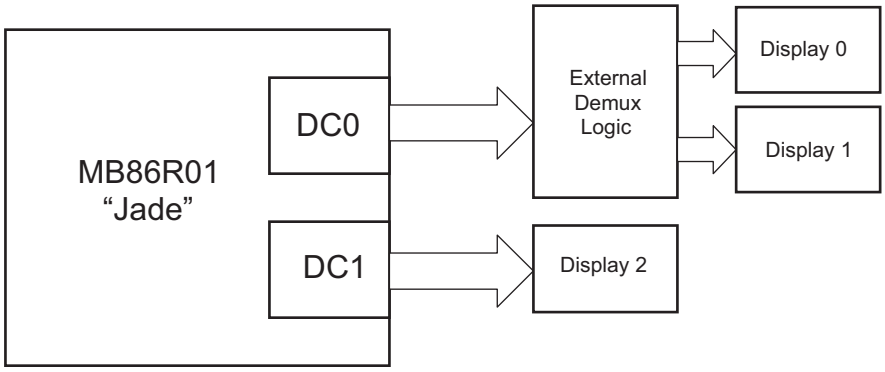

Figure 1. Block Diagram for Display Connections (DC = Display Controller)

MB86R01 "Jade" Display Controller Settings to Enable Multiplex Dual Mode for **Displays 0 and 1**

The relevant details are already listed in section 16.6.11 of the MB86R01 "Jade" GDC Manual rev 1.0. The key points are summarized below.

The multiplex mode can be enabled either in single-edge or bi-edge mode. "Edge" refers to the positive and negative transition of the display clock. The external demultiplexing logic needed to separate the RGB data depends on which mode is selected. An example of the demultiplexing logic and timing for each mode is shown in Figure 2.

Single-Edge Multiplex Dual-Display Mode

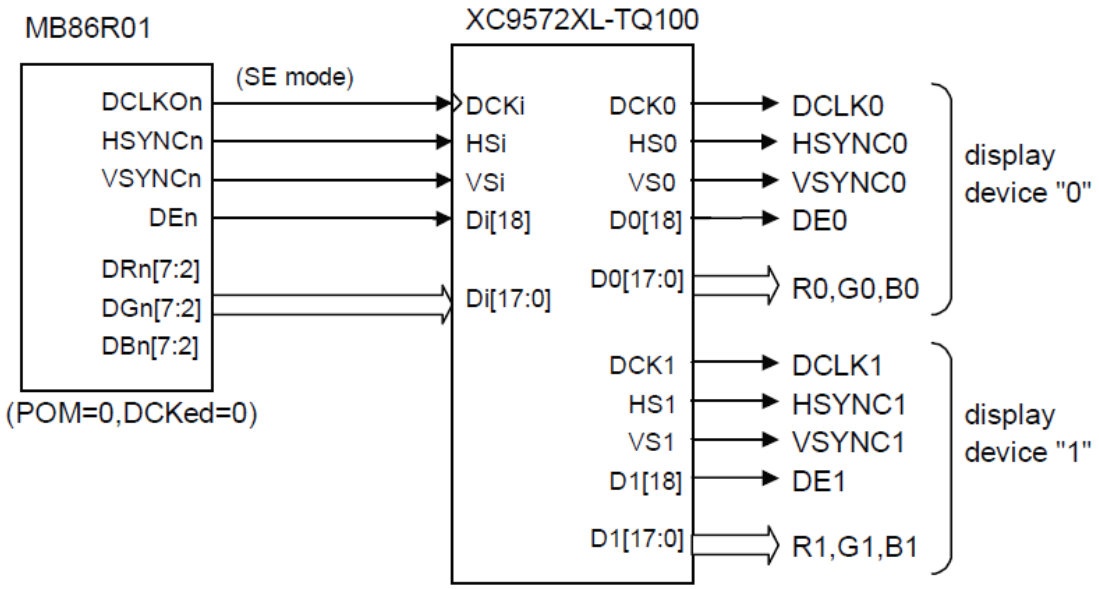

Figure 2 Block Diagram for Demultiplexing Logic in Single-Edge Mode

The demultiplexing hdl code is as follows:

```
module XC9572XL ( DCKi, HSi,VSi,Di,  DCK0,HS0,VS0,D0,  DCK1,HS1,VS1,D1 );
    input DCKi,HSi,VSi;
    input[18:0] Di;
    output DCK0,HS0,VS0, DCK1,HS1,VS1;
    output[18:0] D0,D1;
    reg HS0,HS1, VS0,VS1, DCK0,DCK1;
    reg[18:0] D0,D1;
    always @(posedge DCKi) begin
        HS0 <= HSi; HS1 <= HS0;
        VS0 <= VSi; VS1 <= VS0;
        DCK0 <= (HS0&!HSi)? 0: !DCK0; // sync to ref edge : flip
        DCK1 <= DCK0;
        if(DCK0) D0 <= Di;
        if(DCK1) D1 <= Di;
    end
endmodule
```

Figure 3 shows the resulting output timing diagram for single-edge multiplex dual-display mode:

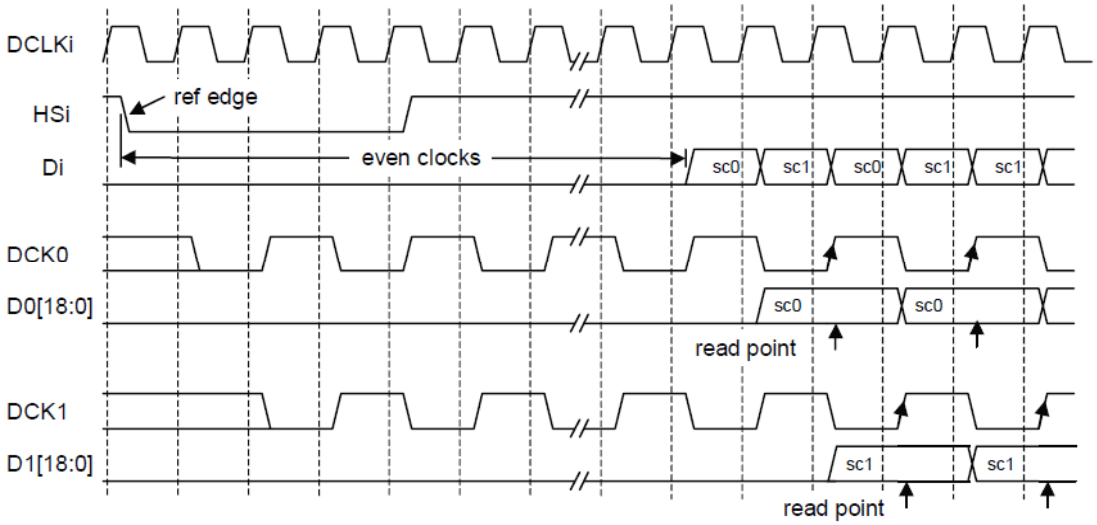

Figure 3.Timing Diagram for Single-Edge Multiplex Mode

Bi-Edge Multiplex Dual-Display Mode

The block diagram for bi-edge mode is shown in Figure 4:

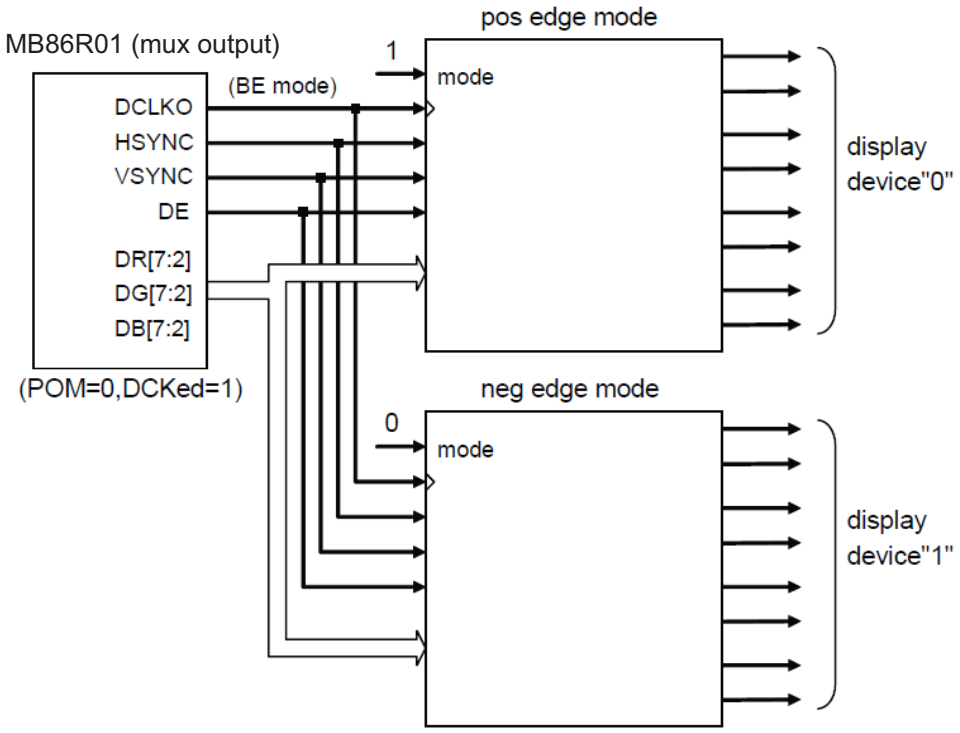

Figure 4. Block Diagram for Demultiplexing in Bi-Edge Mode

Figure 5 shows the resulting output timing diagram for bi-edge multiplex dual-display mode:

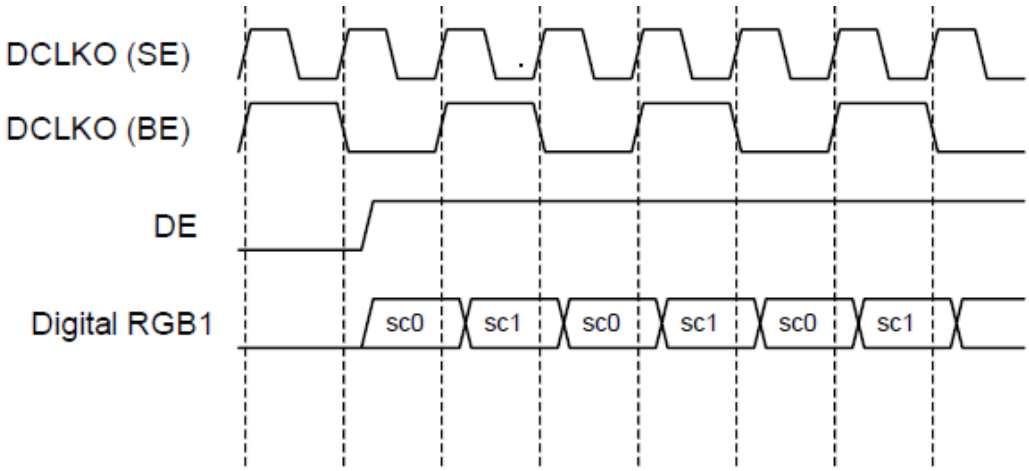

Figure 5. Timing Diagram for Bi-Edge Multiplex Mode

The registers to control the multiplex dual-display mode are DCM3 (bits DCKed and POM) and MDC. Please refer to the MB86R01"Jade" GDC Manual for a full description of these registers. They are found in the"Display Controller Register" section. The division of graphics between the two multiplexed displays is handled by assigning layers to one display or the other. The control for this is provided via the MDC register bits.

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