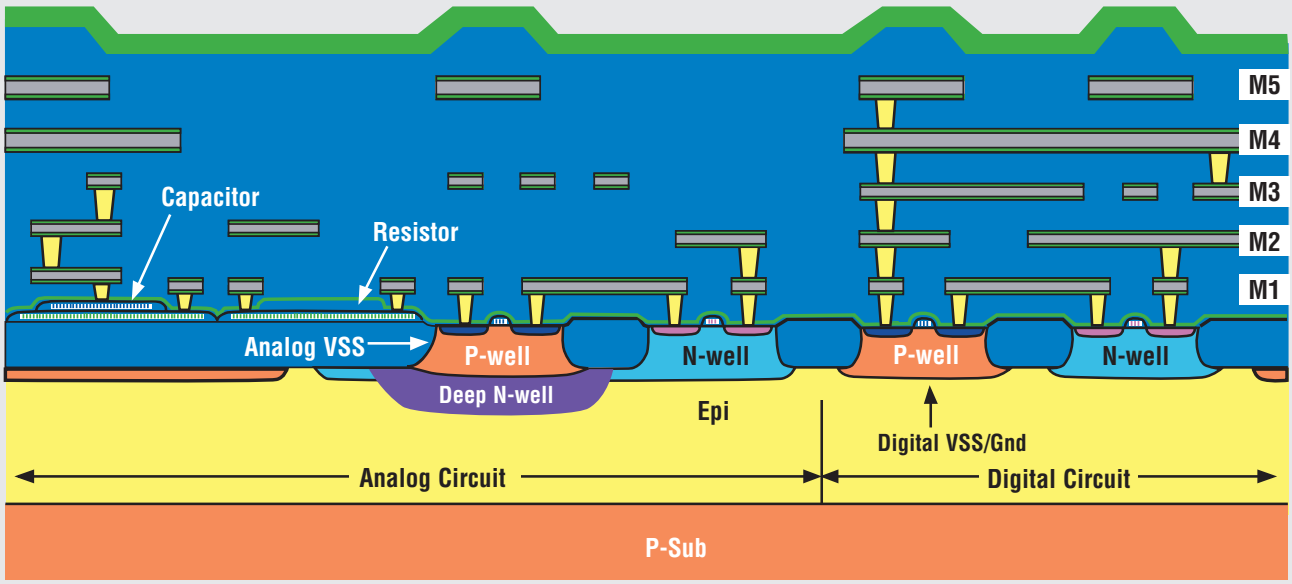
ASIC Mixed-Signal and Analog Macros



Features

- Leading-edge 0.25µm, 0.18µm, 0.13µm, 90nm, 65nm technologies, with a choice of standard twin-well or high performance triple-well design
- Well-adapted to Standard Cells and Embedded Arrays, including Embedded DRAM ASIC (0.25µm) products
- A/D converters: 6-bit to 14-bit, 1 MS/s to 550 MS/s
- D/A converters: 8-bit to 12-bit, 1 MS/s to 220 MS/s
- Analog PLLs and other analog functions
- Low power consumption
- Disable pin for reducing power consumption and IDDQ test
- Precision resistors and capacitors for analog designs (see illustration above)

Description

Technology Overview

To achieve the highest level of system integration, Fujitsu offers a variety of analog and mixed-signal macros for customer use in conjunction with its Embedded Arrays and Standard Cell libraries. Data communications, networking, graphics, and digital audio/video are among the applications that can take advantage of these mixed-signal and analog macros. Additionally, embedded RAMs, ROMs, phase-locked loops (PLLs), and other SOC IP cores from Fujitsu's IPWare™ are provided to enable customers to implement system-level solutions on a single chip.

Triple-Well CMOS Process

Fujitsu's triple-well process allows a P-well to be placed inside an N-well, resulting in three types of well structures, as shown in the illustration above. This third type of well is useful for isolating circuitry within it from other sections on the chip by the reverse bias between the N-well and the P-substrate. For mixed-signal designs, where noise injection can be a problem, the analog sections can be completely isolated from the digital section by using this third type of well structure. There is no resistive path between the analog and digital circuit, since the P-well connected to the analog VSS is isolated from the digital VSS/ground by a reverse biased N-well. The triple-well also significantly reduces the capacitive coupling between the analog VSS and digital VSS/ground. Consequently, a high degree of isolation is achieved for sensitive analog circuits from detrimental digital noise sources.

Triple-well enables Fujitsu to design high-precision analog macros, such as the 12-bit DAC, for mixed-signal ASICs. With triple-well, the sensitive analog circuits of mixed-signal ASICs are

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protected from the noise sources of high-speed digital logic blocks. This isolation technique facilitates in positioning digital and mixed-signal blocks in the closest proximity possible, thereby reducing the overall die size.

Design Support

IEEE is involved in an ongoing process to define and standardize a common analog behavioral modeling language, called VHDL-A. Fujitsu will support VHDL-A when it is ratified. Currently, Fujitsu supports the following mixed-signal simulation tools:

Behavioral/Gate Level Simulation

Verilog

- Digital gate level libraries
- Analog macro functional models

VHDL

- Digital gate level VITAL compliant libraries
- Analog macro functional models

Interface Timing Models for STA

Synopsys — Design Compiler and Prime Time

Transistor-Level Simulation

Hspice — Spice netlist and Level 28 and BSIM-3 models

0.18μm Macro Library

D/A Converters	A/D Converters
8-bit: 300 KS/s, 3.3V	7-bit: 420 MS/s, 3.3V
8-bit: 1 MS/s, 3.3V	8-bit: 1 MS/s, 3.3V
8-bit: 50 MS/s, 3.3V	8-bit: 50 MS/s, 3.3V
10-bit: 300 KS/s, 3.3V	8-bit: 80 MS/s, 3.3V
10-bit: 1 MS/s, 3.3V	10-bit: 1 MS/s, 3.3V
10-bit: 40 MS/s, 1.8V diff.	10-bit: 30 MS/s, 3.3V
10-bit: 50 MS/s, 3.3V	10-bit: 80 MS/s, 1.8V diff.
10-bit: 80 MS/s, 1.8V diff.	
10-bit: 110 MS/s, 3.3V diff.	
10-bit: 110 MS/s, 3.3V	
10-bit: 200 MS/s, 1.8/3.3V diff.	
12-bit: 200 KS/s, 3.3V	
12-bit: 1 MS/s, 3.3V	
12-bit: 110 MS/s, 3.3V	
16-bit: 8-48 KS/s, 3.3V	

90nm Macro Library

D/A Converters	A/D Converters
8-bit: 300 KS/s, 3.3V	6-bit: 108 MS/s, 3.3V
8-bit: 1 MS/s, 3.3V	7-bit: 550 MS/s, 1.2V diff.
10-bit: 300 KS/s, 3.3V	8-bit: 12.5 MS/s, 3.3V
10-bit: 1 MS/s, 3.3V	8-bit: 54 MS/s, 3.3V
10-bit: 45 MS/s, 3.3V diff.	8-bit: 160 MS/s, 1.2V diff.
10-bit: 110 MS/s, 3.3V	10-bit: 1 MS/s, 3.3V
10-bit 220 MS/s, 3.3V	10-bit: 4 MS/s, 3.3V
12-bit: 54 MS/s, 3.3V	10-bit: 30 MS/s, 3.3V
16-bit: 8-48 KS/s, 3.3V	10-bit: 40 MS/s, 3.3V diff.
	10-bit: 80 MS/s, 3.3V diff.
	10-bit: 80 MS/s, 1.2V diff.
	14-bit: 75 MS/s, 3.3V diff.

65nm Macro Library

D/A Converters	A/D Converters
8-bit: 300 KS/s, 3.3V	8-bit: 54 MS/s, 3.3V
8-bit: 1MS/s, 3.3V	10-bit: 1 MS/s, 3.3V
10-bit: 300 KS/s, 3.3V	10-bit: 33 MS/s, 3.3V
10-bit: 1 MS/s, 3.3V	10-bit: 80 MS/s, 3.3V diff.
10-bit: 54 MS/s, 3.3V	10-bit: 90 MS/s, 1.2V diff.
10-bit: 160 MS/s, 3.3V	
10-bit: 220 MS/s, 3.3V	
12-bit: 54 MS/s, 3.3V	

Other Analog Macros in ASIC

Phase-Locked Loops (PLLs) Analog: up 25MHz to 3.2GHz

Op-amps: General-purpose, low noise, high speed, unity-gain buffer, and speaker amplifier

Bias and Vref Circuits: Various kinds, including high stability band gap reference

Analog Switches: General-purpose, 1-ch, 1-ch inv, and 2-ch

Delay Locked Loops (DLLs): 20 MHz to 800 MHz

Comparators: High-speed general purpose

Fuses: Detectors and bias circuits

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