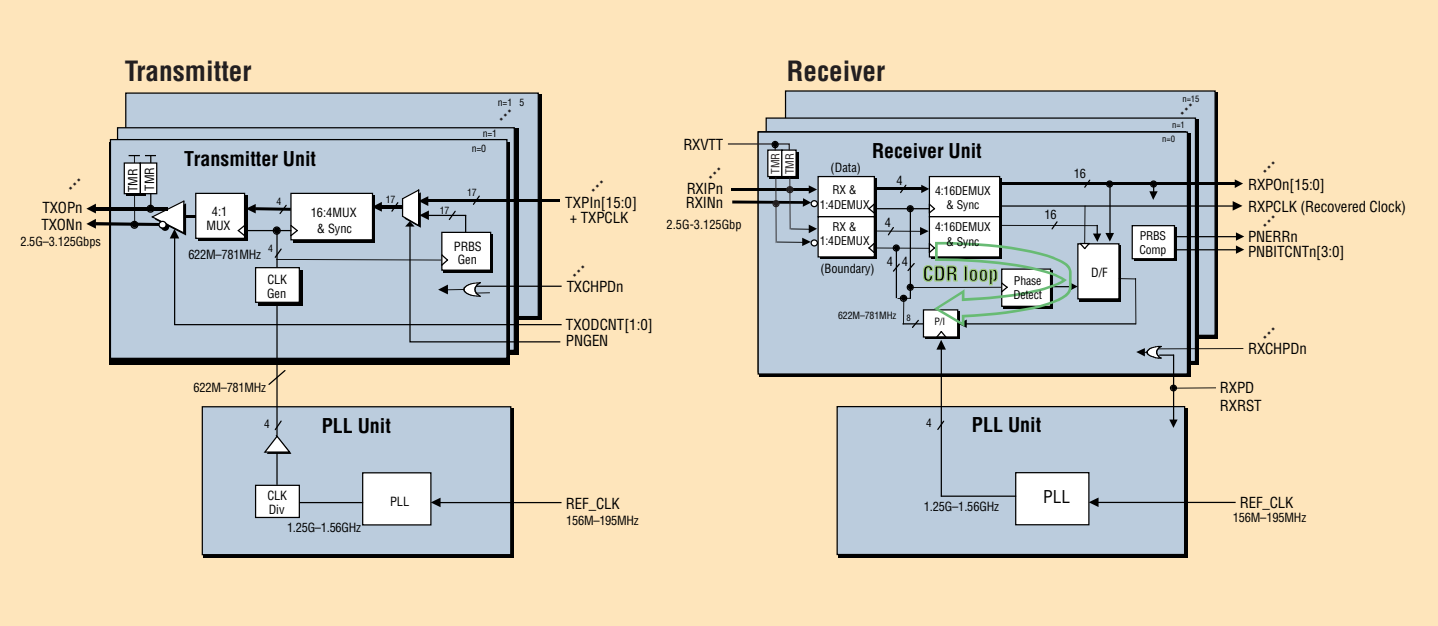
3.125Gbps Parallel CDR Transceiver (0.18µm)



Features

- 2.5Gbps–3.125Gbps per channel unidirectional data transfer rate
- 156 to 195MHz input reference clock and parallel interface
- Available in 2/4/8/16-channel width CDR Rx and Tx arrays for back-plane applications
- Differential PCML (Vterm=1.8V in case of DC coupling)
- AC and DC coupled differential interface
- 1:16 SERDES
- On chip integrated 50-ohm termination resistors
- Independent dual loop PLL and PI (phase interpolator) based CDR on each Rx channel
- Built-in PRBS (2^23-1) generators and comparators for loopback testing
- 1.8V and 3.3V power supply, 0.18µm standard CMOS process

Benefits

- Available as library cell for ASIC designs
- Pre-emphasis based Tx pre-equalization allows up to 12dB high frequency loss
- Programmable Tx voltage swing and amount of pre-emphasis

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Description

Fujitsu's parallel transceiver, which is available in 2/4/8/16-channel width CDR receiver and transmitter arrays, is for ASICs that perform at high bandwidth data communications.

The macro meets SONET/SDH OC-48 jitter tolerance mask requirement. The macro has 175mW/ch power dissipation (including Rx, Tx, CDR, bias circuit and PLL, maximum pre-emphasis, 16ch case) and runs under power supply of 1.8V±0.15V, 3.3V±0.30V and junction temperature of -40°C ~ 125°C.

The macro is fabricated in Fujitsu's standard 0.18µm CMOS technology.

This macro can be used in a variety of applications:

- WAN router or switch backplanes and line card to switch fabric interface
- Any backplane link for 2.5 ~ 3.125Gbps data rate

Deliverables

The Fujitsu value-added 3.125Gbps Parallel Transceiver Macro enables our customers to design a variety of complex system-on-a-chip ASIC designs for high end networking applications.

A Fujitsu application engineer works with the customer to identify the customers' specific IP requirements. Fujitsu will provide the customer with the following information to support the 3.125Gbps Transceiver macro:

- Verilog Model
  - Front-end simulation
  - C model with Verilog wrapper
- Design Compiler Model
  - Timing analysis
- Library Exchange Format (LEF)
  - Floorplanning
  - Place and Route

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