SoC Design Environment RDF V3.0 that Supports Low-power Designs

FUJITSU has released the industry's first design flow RDF V3.0 for ASIC/ASSP that supports the standard power supply description format CPF to facilitate low-power LSI design.

* CPF: Common Power Format

Introduction

Recently, the demand for low power consumption LSIs has been increasing constantly. In concurrence with process miniaturization, the leak current emitted while the transistor is OFF has been increasing and has now reached a level where it can no longer be ignored in products in which battery lifetime is important, such as mobile products.

In this context, FUJITSU has released RDF V3.0, which includes a function to facilitate low-power design in our conventional LSI Design Flow RDF. This article introduces the low-power technology supported by RDF V3.0.

Low-power Design Technology Utilized in an LSI

The types of power consumed by an LSI can be classified into two primary groups. The first is the power consumed during operation; it is consumed as the clock is supplied and the LSI operates. The second is the standby power consumption that is consumed when power is supplied, even when the LSI is not operating. This results from the current that leaks even when the transistor is OFF (leak current)-it was not previously considered a problem in 130nm to 180nm or preceding technologies. Nevertheless, due to the miniaturization of processes, this power can no longer be ignored (**Fig.1**).

In low-power designs, both types of power must be reduced. "Clock gating" and "multiple power supply design" are effective in reducing the operating power consumption and "multi-Vth design" and "power gating" are effective in reducing the standby power consumption.

Clock gating

Clock gating is a conventional technology in which the operating power consumption is reduced by partially stopping clock supply to the resister when it is known beforehand that the input of the register (FlipFlop) will not transition (local clock gating) or by stopping clock supply to suspended blocks (global clock gating) (**Fig.2**).

Multiple power supply design

Multiple power supply design can be used to reduce operating power consumption and standby power consumption (leak current) by supplying multiple power supplies with different voltage levels and supplying low power supply voltage to blocks with low operation frequencies. Areas with different

Figure 1 Leak Current

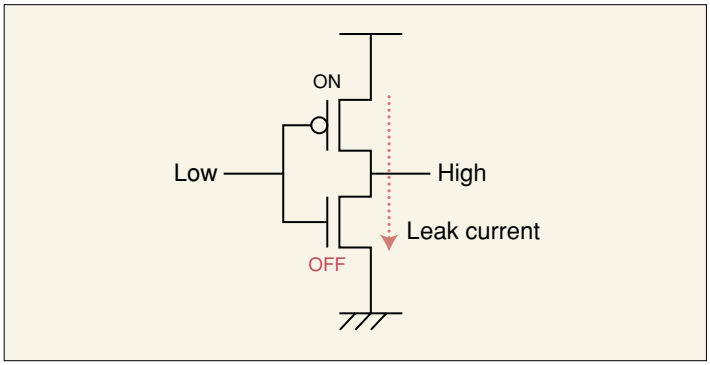


Figure 2 Clock Gating

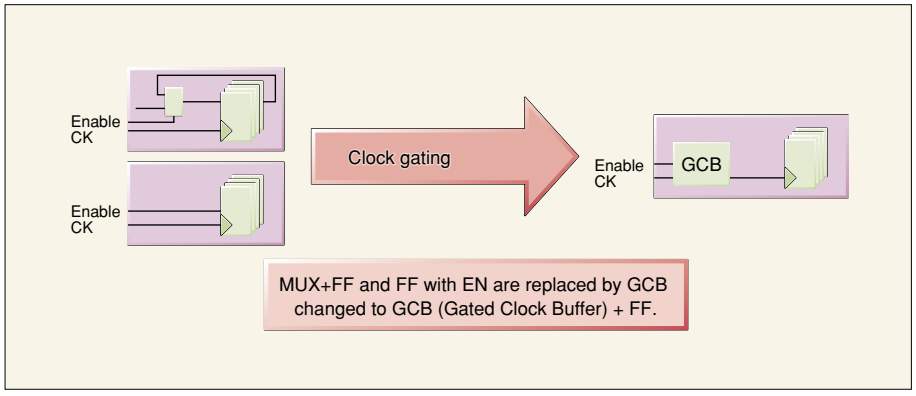


Figure 3 Multiple Power Supply Design

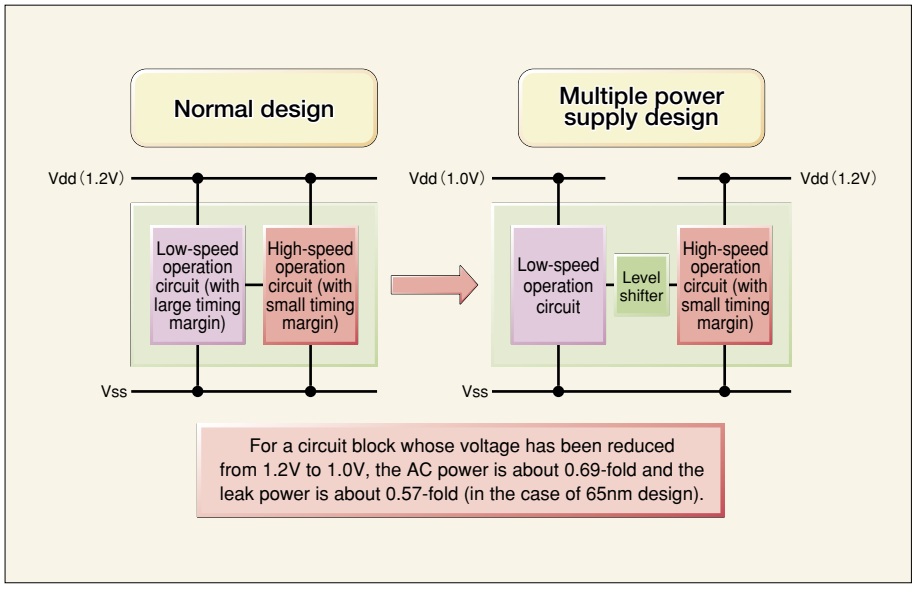
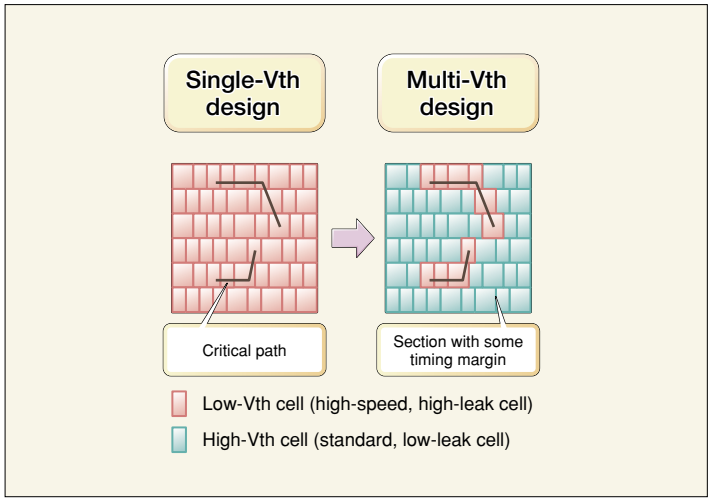


Figure 4 Multi-Vth Design



voltages must be designed physically separate from one another and a cell called a level shifter must be inserted to enable the interface signals between them to convert the signal level (**Fig.3**).

Multi-Vth design

Multi-Vth design is another conventional technology in which the leak current is optimized while satisfying the timing constraint by efficiently using the standard cells consisting of transistors with high speed and relatively large leak current in paths with critical timings and the standard cells consisting of transistors with low speed but small leak current in non-critical paths (**Fig.4**).

Power gating

Power gating is a technology that has been gaining popularity in recent years. It dramatically reduces the leak current by shutting off the power supply to suspended blocks. The method which has switches to shut down the power supply in an LSI is called "on-chip power gating" (**Fig.5**).

Similar to multiple power supply design, the block to shut down the power supply is designed physically separate from others. In addition, since signals from a block with power supply shutdown may be in neutral state that is not high or low, these signals as they are must not be received by operating circuits. A circuit called an isolator must be inserted for such an interface (**Fig.6**).

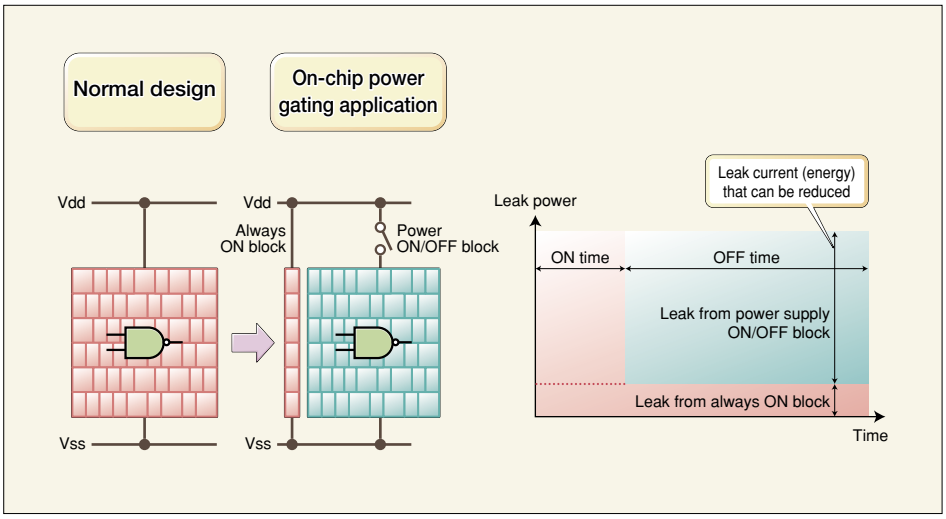
Caution is also required in logic verification. Since the conventional logic simulator cannot handle the status of power supply shutdown, a risk exists that a bug is not found in which the power supply is not actually supplied to a circuit that appears to be operating on logic simulation (**Fig.7**).

Furthermore, the power supply noise generated when the power supply shutdown switch turns ON needs to be suppressed to a level that does not affect other circuits when adopting on-chip power gating (**Fig.8**).

Standard Power Supply Description Format CPF

Although the designer did not need to make special

Figure 5 On-chip Power Gating



consideration regarding the power supply in conventional logic design, it is essential to carefully consider it with multiple power supply design and power gating. Previously, there was no format for power supply description but in 2006, Cadence in the U.S. called for the formation of the Power Forward Initiative (PFI) with approximately 20 corporations, including semiconductor vendors (such as FUJITSU) and EDA vendors. They developed the power supply description format known as the Common Power Format (CPF).*1

As RTL and SDC played roles and expressed logic and timing, respectively, CPF can describe LSI power supply information and the rules for the automatic insertion of a level shifter and isolator. This means, the designer do not need to modify the existing RTL for power gating or multiple power supply (such as inserting power SW and so on).

CPF can realize high-quality design flow with consistent reference in all design phases from RTL simulation to logic synthesis, physical design, and physical verification.

Furthermore, making the logic simulator NC-Verilog (IUS) read the CPF has enabled to check for the bug as shown in Fig.7 in power supply shutdown, which was impossible in conventional settings.

**1: Currently standardized by Si2.*

RDF V3.0 Supporting CPF

In our RDF V3.0, the physical design of multiple power supply design and power gating has been facilitated dramatically by supporting the standard power supply description format CPF ahead of others in the industry.

In addition, highly reliable design can be realized by sharing the single power format CPF with the entire flow, since CPF is described and verified by the logic designer as a GOLDEN information.

Fig.9 presents the overall design flow. Although the over view of the flow is the same, a new function has been added to each step. For example, an appropriate delay calculation is executed to suit the voltage for each power supply area (Power Domain) in logic synthesis, layout, and sign-off verification. Automatic placement clock tree generation, and timing optimization are executed in the layout with consideration given to the physical areas of the Power Domain while the level shifter (LS), isolator (ISO), and power shutdown switch (PSW) are also automatically inserted. The proper insertion of these level shifters, isolators, and power switches is checked by the newly introduced low-power checker,"Conformal-LP." The IR Drop analysis and LVS verification including the PSWs, LSs and ISOs are also supported in RDF V3.0 flow.

Figure 6 Isolator

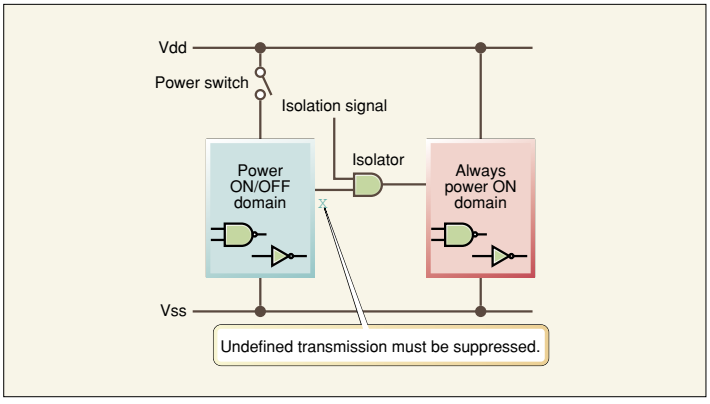
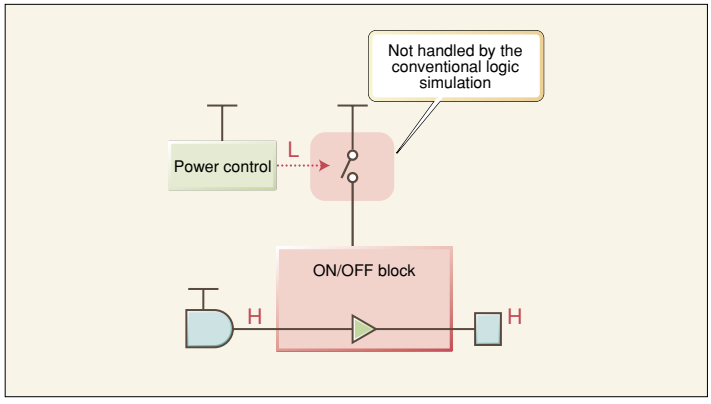


Figure 7 Power Supply Shutdown Bug



FUJITSU has also developed an original power supply switch control circuit (PMU) and the method to adjust the switch parameters to reduce the noise generated when the PSW is turned ON. Using this technology, it is possible to operate on-chip power gating products with more stability. *2

*2: *Patent pending*

Future Developments

As a similar standard format for power supply description to CPF, UPF has been developed by U.S. Synopsys, Mentor Graphics and so forth. To support our ASIC customers utilizing logic design tools by Synopsys or Mentor Graphics, we will support to import the UPF format in 2008 as well.

Summary

RDF V3.0 enables simple and safe low-power design, as shown in **Tables 1** and **2**, through adoption of the standard power supply description format CPF. ✱

Figure 8 Power Supply Noise by the Switch

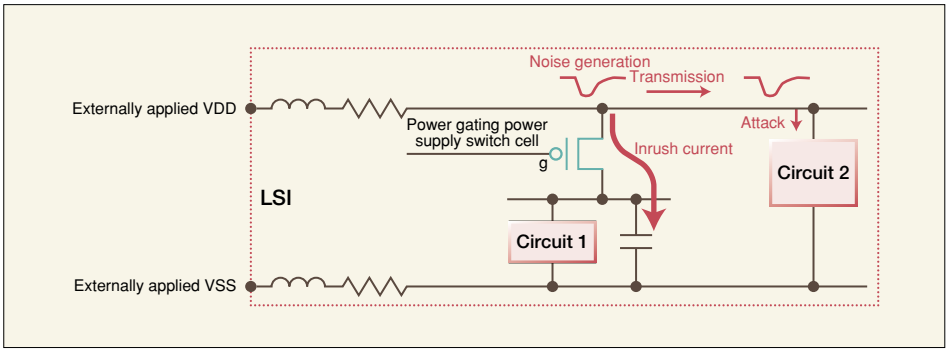


Figure 9 Design Flow

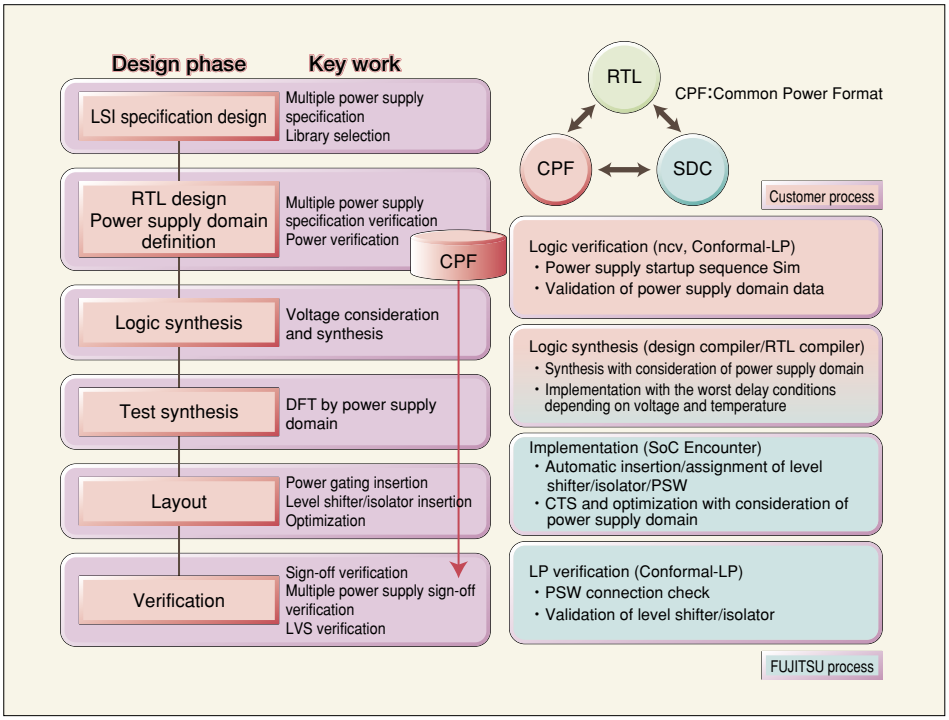


Table 1 Low-power Design Technologies Supported by RDF V3.0

Clock gating	○
Multiple power supply design	○
Multi-Vth design	○
Power gating	○

Table 2 Details of Low-power Design Functions Supported by RDF V3.0

Multiple power supply design	Automatic level shifter insertion	○
	Delay calculation depending on the voltage	○
Power gating	Automatic isolator insertion	○
	Automatic power switch insertion	○
	Power switch noise reduction	○*1
	IR-Drop analysis including power switch	○
	Insertion of always ON buffer*2	○
	Support for retention register*3	In planning
	Logic simulation of power supply shutdown	○
Common	Check on level shifter/isolator omission	○
	Calculation of power consumption	○
	Physical verification (DRC, LVS)	○
	Support for UPF	In planning

∗1:This technology is for ASIC/ASSP. To support COT customers, a support or development charge will be required separately.
∗2:A special repeater buffer cell used for wiring that needs to pass over the power supply shutdown area.
∗3:A special FlipFlop with a saving latch to maintain the value even during power supply shutdown and a second power supply terminal.