High-speed Interface Technology for Image Data Transmission

It is now possible to handle high-resolution data in consumer products such as full HD flat-screen TVs. As such, the transmission of large volumes of data between and inside these devices is required. However, various problems have arisen in data transmission using the legacy CMOS interface, revealing its limits. This article presents various high-speed interface technologies that are beginning to be adopted in order to replace it.

Advantages of high-speed signal transmission

Reduction in signal lines and system cost

For example, to transmit 8.0Gbps data, the number of signal lines required is calculated as follows:

For a CMOS interface (75MHz),

8Gbps/75MHz=107 lines (single ended)

+14 lines will be required to run 1 source synchronous clock for each of the 8 data lines; thus, a total of 121 lines is required.

For a high-speed interface (2Gbps, LVDS),

8Gbps/2Gbps×2 (differential)=8 lines

Thanks to the embedded clock (CDR), it requires no clock line, which enables a reduction of more than 100 signal lines.

The number of power supplies and grounds for the interface can also be reduced. Overall, approximately 150 lines are reduced if the power supply / ground for singnal line ratio is 1 : 2.

With this reduction in the number of signal lines, power supplies, and grounds, cost reduction is possible for transmission lines between LSIs (printed circuit board, cables, and connectors) as well as for the LSI itself (package and chip).

Measures against noise

When many signals change simultaneously, switching noise of V=−L di/dt occurs due to rapid current change and the package inductance in legacy CMOS interfaces—depending on the amount of noise, this can lead to data error (noise due to SSO[*1]). Reinforcement of the power supply and the ground is necessary to mitigate this problem.

High-speed interfaces use differential signals and circuits with small changes in power supply current such as LVDS or CML. Furthermore, the differential signal transmits in "normal" and "inverse" phases, and is also effective as a measure against EMI since the electro-magnetic field is coupled among signals and the radiation noise leakage to the exterior is reduced.

Reduction in power consumption

Power consumption can be reduced compared to transmission by CMOS. For example, it can be calculated as follows in the aforementioned case:

- CMOS: 107 lines×3mW (3.3V, 75MHz, 10pF)=321mW
- LVDS: 8 lines×6.6mW (100-ohm, 200mV) =53mW

This enables simple power supply and thermal designs and leads to package and chassis cost reduction.

Increased Necessity for High-speed Signal Transmission in Consumer Devices

Improved image quality is demanded in consumer devices that handle images such as digital still cameras and digital TVs. To satisfy this demand, resolution and frame rate are being increased dramatically compared to conventional levels.

For example, digital TVs have shifted from the conventional 480i (SD, 4 : 3, vertical resolution 480 lines, interlace, 30fps[*2],

24-bit color) to 1080p (full HD, 16 : 9, vertical resolution 1080 lines, non-interlace, 60fps, 30-bit color) in concurrence with full HD adoption. This is calculated in terms of data volume as follows:

- 480i: 480 (V) × 640 (H) × 30 (fps) × 24 (bit) = 0.22Gbps
- 1080p: 1080 × 1920 × 60 × 30 = 3.73Gbps

(V: Resolution in the vertical direction, H: Resolution in the horizontal direction)

Approximately 17x data transmission speed is required.

In conventional SD, a CMOS interface was used for this data transmission. The transmission of 480i data in three CMOS interfaces can be calculated as follows and data transmission is feasible:

- 0.22Gbps/3 lines = 74Mbps/line

However, when full HD 1080p data is transmitted via the same CMOS interfaces, it is calculated as follows:

- 3.73Gbps/74Mbps = 51 lines

Furthermore, approximately 60 lines will be required including the parallel source clocks.

There will be problems such as skew matching between clock and data, SSO noise, and EMI noise when transmitting a 74Mbps signal with CMOS interfaces in 50 or more lines.

There is a demand to increase the refresh rate from 60fps to 120/180/240fps (2x, 3x, and 4x speeds) to improve the image quality. These data rates will require 100- to 200-line transmission, which is not feasible in terms of cost and power consumption when the LSI pin number, package, printed circuit board, connector, cable, and so forth are included.

Therefore, instead of increasing the number of lines, high-speed interfaces that increase the data transmission rate per line are adopted.

For example, when the frequency is increased 7x for 1080p data, it is calculated as follows:

- 3.73Gbps/(74Mbps × 7) × 2 (differential) = 14.5 lines

* *However, the amplitude needs to be reduced for high-speed transmission and differential transmission must thus be adopted. Two lines per signal will be required.*

The problems of SSO noise and EMI noise are reduced dramatically compared to the legacy CMOS interface thanks to the natures of the previously described differential transmission and circuit (LVDS, etc.).

High-speed interfaces have been used for similar reasons in devices that handle large volumes of data (telecommunication devices, servers, etc.). This technology is currently being used in consumer devices as well.

Utilization in each application field

Digital still cameras (DSC) (Fig.1)

Digital still cameras require large data bandwidths for transmission from the image pickup device to the image-processing chip.

The number of pixels for the image pickup device has increased to between 5M (5 million) to 12M range in compact digital cameras.

- 5M (pixels) × 10-bit × 15fps = 0.75Gbps

15fps is used for live viewing (viewing of the shooting image on the LCD screen). When the number of pixels and the frame rate increase, the data rate increases dramatically. For example, 12M pixels at 30fps requires the following data rate:

- 12M × 12-bit × 30fps = 4.32Gbps

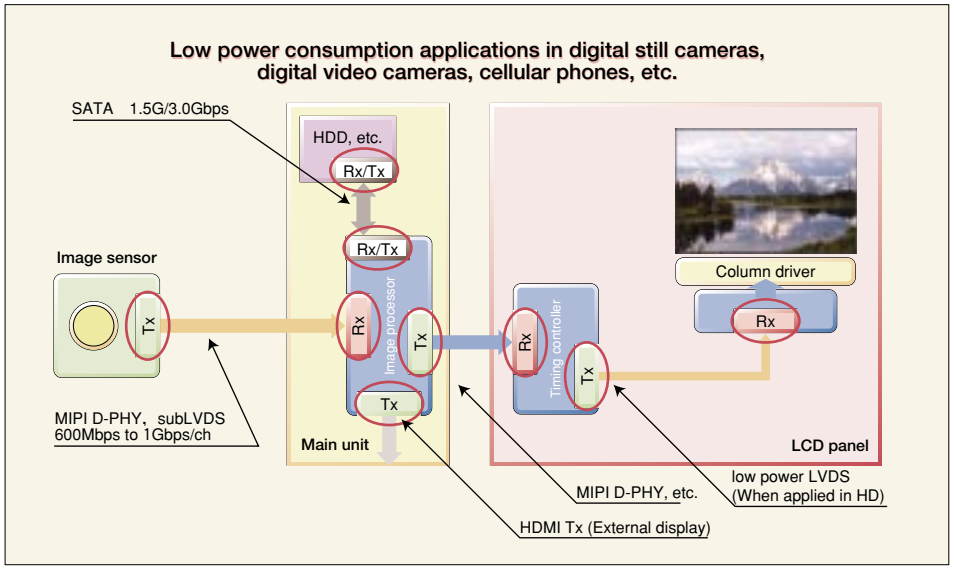
It is expected that EVF[*3] will be used in high-end digital cameras in the future. In this case, a large number of pixels as well as a smooth display of motions will be required, leading to the transmission of larger volumes of data. When data is transmitted for 24M pixels at 16-bit 60fps, it is calculated as:

- 24M × 16-bit × 60fps = 13.44Gbps,

which is a data volume that requires 14 sets of 1Gbps interfaces.

For these differential transmission interfaces that minimize the amplitude and power supply voltage thus reduce the power consumption compared to the

Figure 1 High-speed Interface in Mobile Applications



conventional LVDS, such as CCP2[*4] subLVDS and MIPI D-PHY[*5] are now used in recent models (**Fig.2**).

Table 1 presents a comparison among high-speed interfaces with low power consumption. MIPI D-PHY, which is capable of reducing the power supply voltage, is advantageous in terms of power consumption.

Furthermore, some devices are beginning to equip HDMI outputs compared to the conventional products with only analog video outputs (**Fig.3**). While HDMI requires 3.3V termination, the load on the transmitter side is not an issue, since the power is supplied to the terminating resistor from the receiver side.

Digital video cameras (DVC) (Fig.1)

The data rate exceeds 1Gbps due to adoption of high definition (HD) at 1080i/1080p and so forth, increased number of frames, and increased bit number per pixel to improve the image quality.

- 2M ×12-bit ×60fps =1.44Gbps (1080p, 12-bit, 60fps)

Since the data stream from image pick-up device is written into the storage with compression in digital video cameras, the required data transmission rate is not very high. HDD and Flash memory cards are currently used as the storage, with interface shifting to SATA and so forth (**Fig.4**). When the video data accumulated in these are to be transmitted to PC and other devices, the current USB2.0 (480Mbps) interface will require several ten minutes. Thus there is a demand for higher transmission speeds. Standards such as USB3.0 with 10x speed (5 Gbps) are currently being developed, and it is expected that the interfaces will shift to these in the future.

Cellular phones (Fig.1)

The basic configuration of image-related interfaces is the same as DSC and DVC. The number of pixels in built-in cameras in cellular phones is also expected to increase from 5M pixels to 8M and then to 12M in the future.

- 5M pixels ×15fps ×10-bit =0.75Gbps
- 12M pixels ×30fps ×12-bit =4.32Gbps

Table 1 Comparison of High-speed Interfaces with Low Power Consumption

	LVDS	subLVDS	D-PHY
Speed	Up to 1Gbps	Up to 650Mbps	Up to 1Gbps
Power supply voltage	2.5 to 3.3V	1.8V	1.2 to 0.8V
Amplitude	0.4V	0.4V	0.2V
Common mode voltage	1.2V	0.9V	0.2V

Figure 3 90nm HDMI Tx (Transmission) Macro

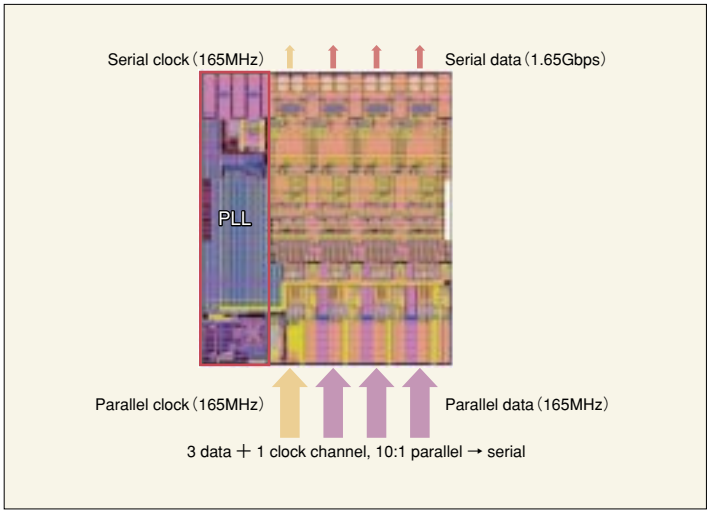


Figure 2 90nm MIPI D-PHY I/O

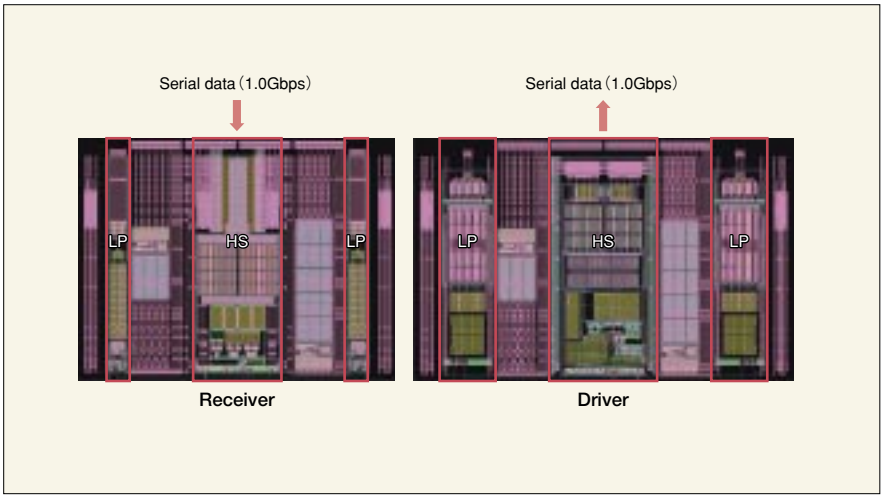
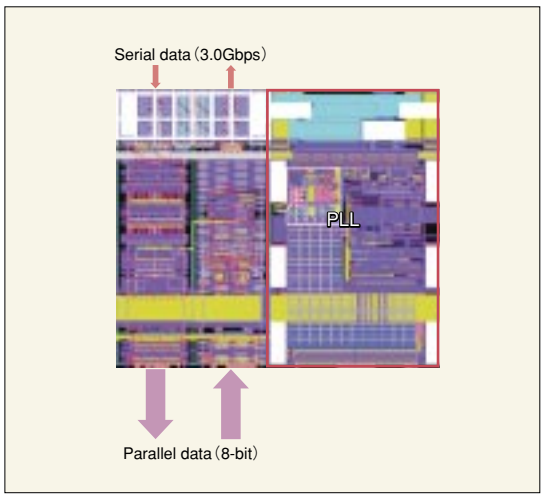


Figure 4 65nm SATA PHY Macro (×1 configuration)



In addition, the displays are currently at VGA level and require only about

- 640 × 480 × 30fps × 10-bit × 3 = 0.27Gbps, but they may require
- 2M × 60fps × 10 × 3 = 3.7Gbps, if HD is adopted in the future with the introduction of laser projectors and so forth, and the data bandwidth required will be equivalent to those of the current digital TVs.

Digital TVs (DTV) (Fig.5)

① Digital signal input (HDMI)

HDMI has become popular as the digital input for digital TVs. Recently, most DVD players also have HDMI outputs. Color depth has increased from the conventional 24-bit to 30-bit, and some are even adopting 36-bit. To address this, interfaces are shifting from 0.8Gbps for 1080i to 1.65Gbps for 1080p or 2.25Gbps to support deep color.

In this transmission architecture, the clock and data are transmitted with frequency synchronization and the mechanism allows some degree of the phase skew at the receiver side. In this way, the skew matching on the printed circuit board or cable is mitigated. Its standard thus supports up to 3.4Gbps.

With a synchronous link composed of LVDS, the transmission path is extremely difficult to design with 1Gbps or higher per line unless there is a mechanism for skew compensation; the cost increases dramatically as well. If there is a circuit to automatically adjust the skew, 3Gbps or higher can be realized, as in HDMI. In this case, there is no need for synchronization with the clock phase, although it is synchronous to the frequency.

Figure 5 High-speed Interface in Digital TV Applications

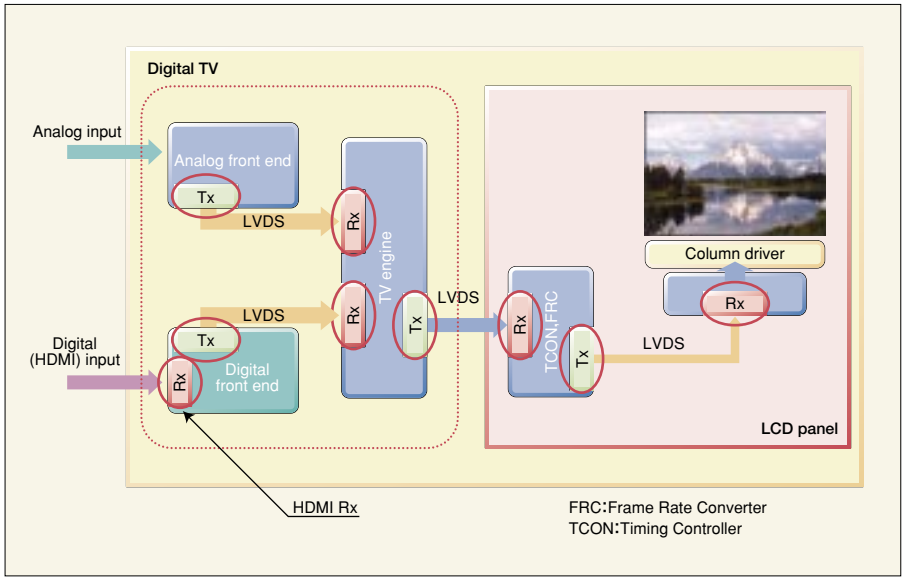
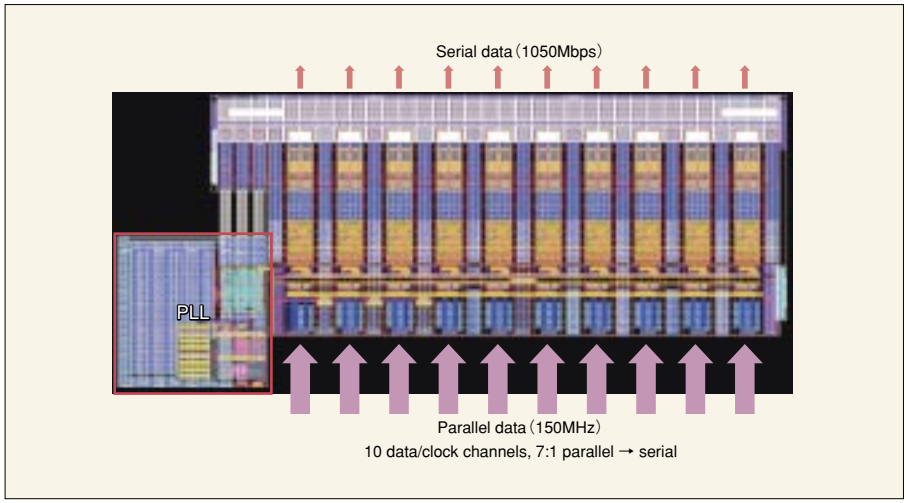


Figure 6 65nm LVDS Tx (transmission) Macro



② Interface to the panel

The data rate has also increased internally for DTV due to increased frame rates. The screen refresh rate (frame rate) has recently increased from the conventional 60Hz to 120Hz. It is expected that 180Hz and 240Hz, which is considered the limit for the human eye, will also be adopted in the future.

In terms of the screen resolution, the current full HD (1920×1080) will be used for some time, but 4k×2k is expected to be adopted depending on the application and 8k×4k will be used in high-end products in the future.

- 1920×1080×60×30 = 3.73Gbps (1080p, 60Hz, 30-bit)
- 4k×2k×120×36 = 28.8Gbps (4k×2k, 120Hz, 36-bit)

At present, the method to transmit with synchronous clock and data using several LVDS links is used. FPD Link is one such method (**Fig.6**).

While data transmission up to about 1,120Mbps has been achieved for data with 160MHz clock per line, skew matching between clock and data becomes difficult as the speed is increased. The current transmission scheme is considered to be nearly at the limit.

This is a similar problem to one that occurred in internal data transmission (backplane) in telecommunication devices more than a decade ago. To solve this problem, adoption of the CDR (clock data recovery) method to use the

embedded clock in data will be inevitable.

At present, DisplayPort*6 adopts this CDR method.

Consideration of the Transmission Path

While inexpensive cables and connectors are becoming popular, their actual characteristics vary widely.

Fig.7 presents the transmission characteristics of SATA cable, and **Fig.8** shows a measurement example of impedance characteristics.

In regard to impedance characteristics (TDR), impedance increases due to large resistance per unit length as the length increases in thin cables. Furthermore, there is a large difference between those with large reflection at the connector section and those with small reflection. It is assumed that this difference is caused by the way in the assembly process of the connectors as well as the difference in the characteristics of the connector itself.

As shown above, the actual characteristics may vary dramatically even if the costs are similar. It is important that the transmission paths be designed appropriately by understanding the transmission characteristics when selecting transmission path parts.

Summary

High-speed interfaces that were previously mainly adopted in telecommunication devices are now beginning to be widely used in consumer devices. By integrating them into an LSI, it will be possible to reduce the system cost while utilizing their features of high speed, low power consumption, and low noise.

High-quality signal transmission can be realized even with inexpensive parts by designing the transmission paths with due consideration beforehand. *

NOTES

*1: SSO: Simultaneously Switching Output

*2: fps: frames per second: screen refresh rate

*3: EVF: Electronic View Finder: A method in which an image is displayed with high resolution with no delay in data from the image pickup device. While an optical viewfinder is currently used for resolution and clarity, it has some disadvantages in that white balance and so forth cannot be distinguished by looking at the finder screen.

*4: CCP: Compact Camera Port: The interface standard for portable cameras developed by SMIA (Standard Mobile Imaging Architecture), an organization promoting the standardization of cellular phone interfaces.

*5: MIPI: Mobile Industry Processor Interface: An organizational alliance promoting the standardization of interfaces used in cellular phones.

*6: DisplayPort: An interface for displays specified by VESA (Video Electronics Standards Association), an organization promoting the standardization of video devices for PCs.

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Figure 7 SATA Cable Transmission Characteristics (S parameter, S21)

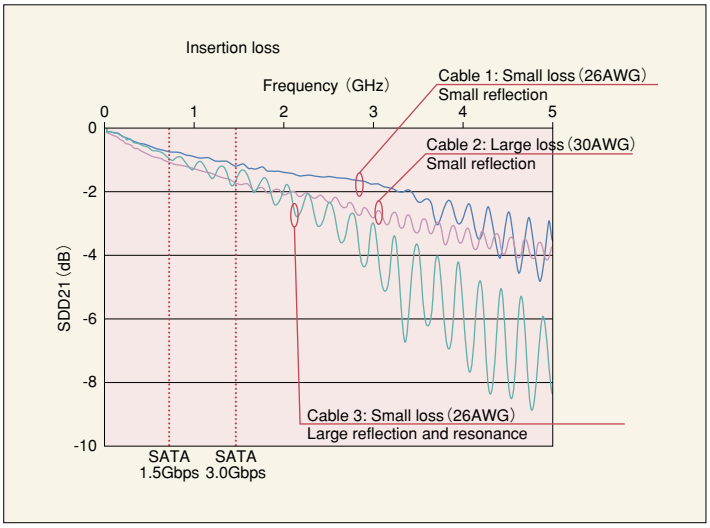

Figure 8 SATA Cable Impedance Characteristics (TDR Measurement)