Fujitsu Semiconductor Europe

Factsheet
FCR4 Cluster SoC Family

Scalable Solution for Hybrid Automotive Instrument Clusters

The FCR4 Cluster family of devices has been especially designed to offer an innovative, scalable solution for hybrid clusters, which combine traditional meters and graphical displays. With their embedded flash, the FCR4 MCUs and SoCs can serve as single-chip solutions or operate as companion chips for other devices to build high performance systems for virtual / free programmable clusters.

FCR4 devices offer a powerful architecture based on the ARM® Cortex™ R4 core and Fujitsu's 2D 'IRIS' graphics engine. They include the required safety and security features, allow for today's requirement for low power consumption and are developed to fulfill highest automotive quality standards.

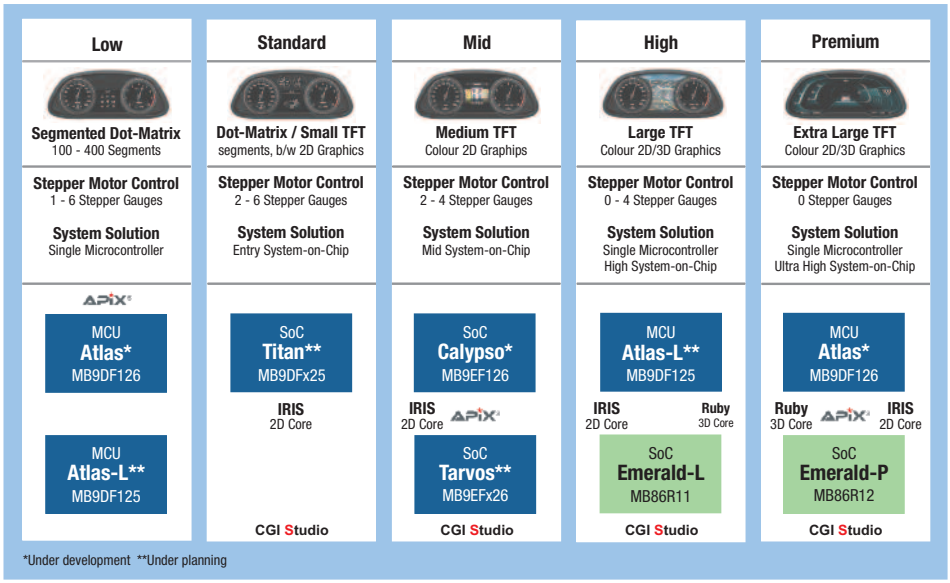


Diagram showing 'Right-Sized Solutions' of FCR4 product range

Features of the FCR4 Cluster Family

Main processor
- ARM Cortex R4
- 1.6DMIPS / MHz
- Up to 16kB I-Cache, 16kB D-Cache
- 160MHz operating frequency

Memories (all with ECC)
- 2MB Flash / 64kB E²Flash
- Up to 208kB RAM

Graphics (depending on device)
- 2D graphics engine IRIS
- Up to 2MB embedded VRAM
- Display controller / TCON
- Signature unit
- Command sequencer
- APIX® 1.0 transmitter

Cluster features
- 6 SMC + Fujitsu ZPD
- Real-time clock / auto calibration
- Sound generator
- I²S

Connectivity
- CAN, LIN, SPI, I²C,
- HS-SPI (memory mapped access)
- Ethernet (10/100)
- External Bus I/F

Safety
- MPU, PPU, TPU, CRC
- Window watchdog
- Error collection unit

Security
- Flash-, Debug- and Test-Security

Low power
- Switchable power domains
- Retention RAM
- Flexible clock control

Other features
- PWM (phase shift, ramp function)
- 10-bit ADC (range comparator)

Debugging / testing
- ARM Coresight Debug and Trace
- Debugging via JTAG Interface
- 8-bit trace / 32-bit full trace via bond-out chip
- Boundary scan

Characteristics
- 5V capable I/Os
- Ta: -40 to +105°C

'IRIS' 2D Graphics Engine

'IRIS' is one of the key features of the FCR4 family and it is included in 'Emerald' as well. 'IRIS' is a modular system of building blocks, which can be combined to find the optimum scalable solution for customer requirements.

IRIS Features

Display controller / TCON
- 4 display layers of overlay
- Video modes up to 40MHz pixel clock (e.g. QVGA, VGA, WVGA)
- TTL/RSDS interface with 12 freely programmable pulse generators
- Programmable phase shift for panel clock
- Horizontal/vertical flip.
- 90/180/270 degree rotation.
- LUT for non-linear correction

Signature unit (Safety)
- per-pixel mask feature

Command sequencer
- DMA operations
- Sub routines
- Synchronisation to 'IRIS' events
- Unloads system CPU
- Memory mapped command FIFO

IRIS Pixel Engine
- Re-configurable concept (functionality can be selected for blit or display)
- Optimised for memory saving
- Freely configurable pixel formats (packed 1, 2, 4, 8, 16, 24, 32 bpp)
- Colour palettes
- Run-length decoding
- Single pass rendering of blit sequence operations (no temporary buffers)
- Bitmap decompression with clipping on the fly (no need to store decompressed bitmap)
- One pass combinations of various operations (no need to store intermediate results)
- Multiple blend operations in one pass (no need to store intermediate results)
- Supported blend modes (constant + alpha, pre-multiplied)
- PixBltBlendLumColor feature (highlighting with const. colour blending – no need to store multiple coloured bitmaps for highlighting)
- Typical example: Rotation, scaling and blending of compressed bitmaps

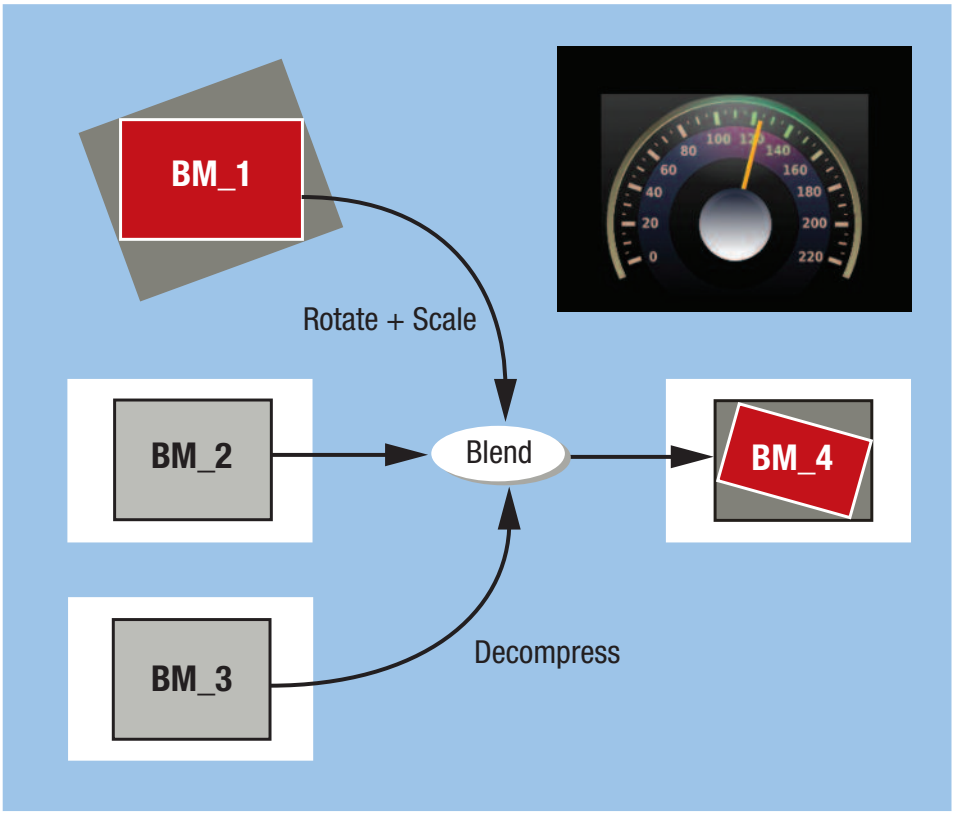


Diagram showing 'IRIS' decompress, rotate + scale and blend 2D bitmaps

'Use Case' example for 'IRIS'

Input
- BM_1: uncompressed
- BM_2: uncompressed
- BM_3: compressed

Operation
- 1st step
  - BM_1 ⇒ Clip + Rotate + Scale ⇒ BM_1*
  - BM_2 ⇒ Clip ⇒ BM_2*
  - BM_3 ⇒ Decompress + Clip ⇒ BM_3*
- 2nd step
  - BM_1* + BM_2* + BM_3* ⇒ Blend ⇒ BM_4

BM = bitmap
* = intermediate result of operation

Notes
- Complete operation without the need to save intermediate results
- BM_1, BM_2, BM_3 need not to have the same colour depth (automatic conversion)
- All OpenGL ES 2.0 and OpenVG blend modes are supported

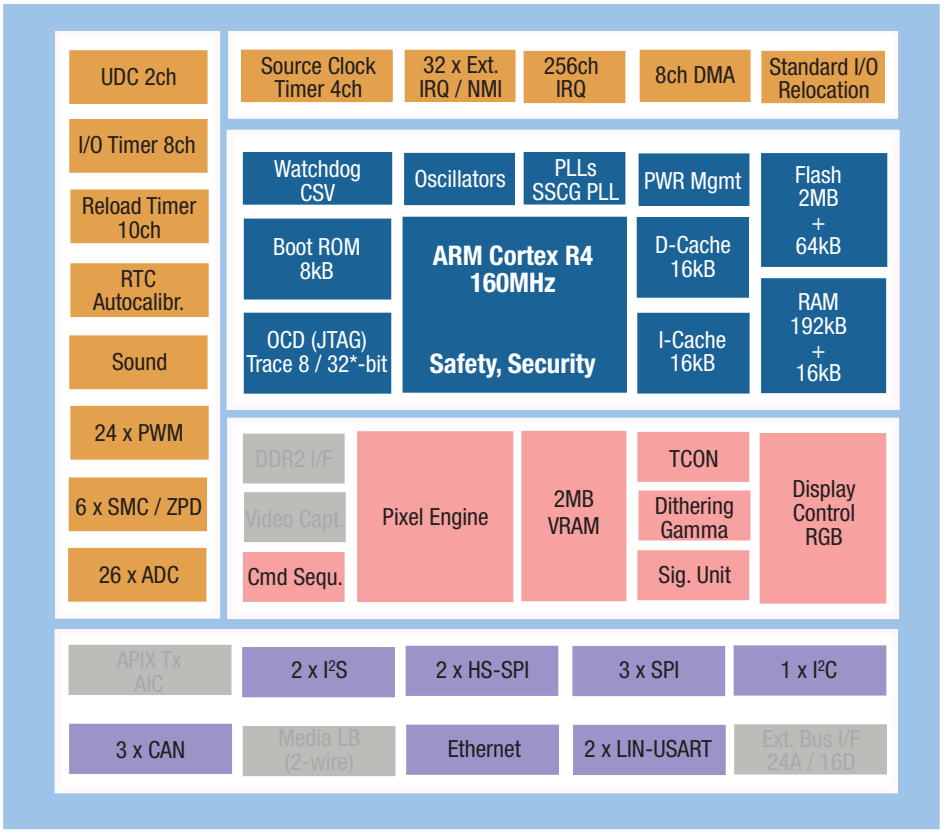
The information on this page relates to the first 2 members of the FCR4 Cluster family - more are under development

'Calypso' MB9EF126

Calypso is designed as a single-chip solution for hybrid automotive instrument clusters. It contains support for up to 6 traditional gauges as well as the 2D graphics engine to drive a graphical display. It contains sufficient Flash, RAM and VRAM for this purpose. For more details see the block diagram:

Key features

- Flash SoC:
  - 2MB flash, 208kB RAM
  - 6 x SMCs
  - 3 x CAN, HS-SPI, Ethernet
  - 2D Engine IRIS, 2MB VRAM
- Package: BGA-320



'Calypso' MB9EF126 block diagram

'Atlas' MB9DF126

As successor to the well known MB91460 cluster MCUs, 'Atlas' can be used as a standalone MCU driving up to 6 SMCs or in combination with other devices to support more complex clusters. For details see the block diagram:

Key features

- Flash MCU:
  - 2MB flash, 208kB RAM
  - 6 x SMCs
  - 3x CAN, HS-SPI
  - APIX Tx (512Mbit/s)
  - External bus
- Package: QFP-176

'Atlas' can serve as a standalone cluster MCU or companion MCU to

- Fujitsu 'Emerald' family
  - ARM Cortex A9 based high-end graphics controller
  - 2D/3D engines
- Fujitsu 'Indigo' family MB88F33x

'Atlas' MB9DF126 block diagram

Tools, Software and Services

In addition to the devices themselves Fujitsu, together with various well-known partners offers the required ECOsystem around the MCUs and SoCs:

BSP software

- Header files, low level libraries, software examples, template project
- Autosar
  - Autosar 3.1 – MCAL Development by Fujitsu Semiconductor Europe
  - Autosar complex drivers:
    - E²PROM emulation
    - APIX remote handler driver
    - More under development
  - Complete Autosar via ecosystem partners

- 'IRIS' graphics driver
  - Simple API
  - Adds additional features like line drawing, filled rectangles

Developer Suite

- Extension of GDC studio to include MCUs
- Quick start-up of and first test of hardware without C-programming
- Flash programming

GDC designer

- 2D HMI design, code creation and preview

CGI Studio

- Same tool environment as for 3D engines
- Visual 2D HMI processing and composition
  - 2D scene composition
  - 2D animation effects (scale, rotate, translate)
  - 2D visual effects for 'IRIS' based GPUs ('Emerald', 'Calypso', ...)

Development tools (compiler, debugger)

- Standard tools (compiler, debugger) from well known 3rd parties
- Standard JTAG Debugger hardware and trace support from well-known 3rd parties
- Ecosystem partners:
  - IAR systems
  - Green Hills Software
  - More on demand

Evaluation boards

- Modular starter kit
  - Base board per device (e.g. SK-MB9EF120-001) with power supply and debug / trace connections / flash i/f
  - Universal I/O extension board (ADA-FCR4-MULIIO-001) with more connectivity
  - Application related extension boards (e.g. ADA-FCR4-CLUSTER-001)
- Trace adaptor per device (e.g. ADA-MB9EF120-001)

Services

- To complement the line-up of hardware and software solutions Fujitsu offers various services on demand. Some examples:
  - Training
  - PCB reviews
  - EMC consulting
  - Software porting

Green Hills SuperTrace Probe v3

IAR J-Link, ARM JTAG Debugger 1

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