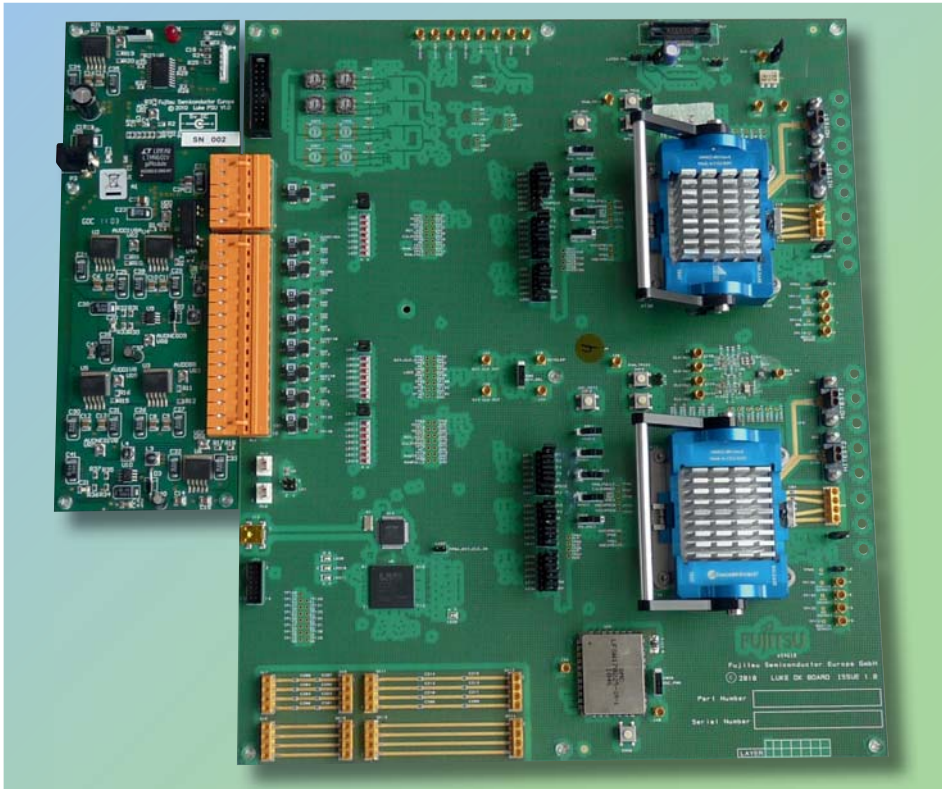


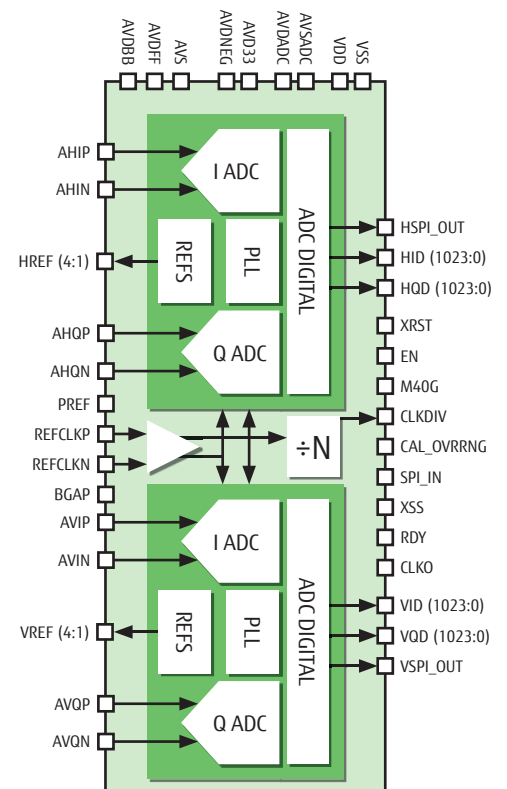
Analog to Digital Converter evaluation board



The 40nm CHAIS ADC evaluation board is intended to allow rapid characterization of the CHAIS ADC test chip. Two variants of the board are available. The first option is mounted with two low inductance sockets which allow rapid replacement of the device under test. The sockets incorporate a heat sink for increased heat dissipation. This can also be used with temperature forcing systems to precisely control the die temperature. The second option of evaluation board has devices mounted directly onto it. Special attention has been given to the connector choice to allow connection to instrumentation which will perform the design verification tests. The printed circuit board utilizes high performance materials to optimize the integrity of the signals. The development board also has a USB interface that allows the device to be programmed through a windows application running on a host PC.

Key Features

- 2 Luke test chips mounted to a high performance printed circuit board giving 2 x IQ pairs (4ch x 55 - 65Gsp/s ADC)
- Superior signal integrity from using low loss materials
- Access to ADC inputs via SMPM connectors
- Software for control of the device from host PC
- Integrated USB interface
- Powered from 100 - 250V ac mains power source
- Integrated clock distribution circuitry
- Option to mount a low inductance socket to allow replacement of device under test
- Dual device synchronisation circuit



Full ADC macro block diagram

Applications

- 40G/100G Communications Systems
- Test Equipment

ADC Macro Features

- Fujitsu 40nm Technology
- Resolution : 8-Bit
- 4 Channels (2 x IQ pairs)
- Sampling Rate : 55 – 65 GS/s
- Power Supply : 1.8V, 0.9V, -0.9V, -1.8V
- Power Consumption : 1.2W/ch
- DNL : ± 1 LSB, INL : ± 3.0 LSB
- ENOB: 5.7 (-6dBFS sinewave at ~8GHz)
- Differential Analog Input : 0.7VPPDiff
- 20GHz -3dB Input Bandwidth
- 2's Complement Data Format
- Output Rate: 128Samples @ 511.9MHz
- 0.9V Data Output Clock @ 511.9MHz
- REFCLK=N programmable output clock
- 1.75 – 2GHz Input Reference Clock
- Internal 13.44 – 16.38GHz Differential VCO
- Self contained background calibration
- Calibration over-range flag
- Designed for Flip-Chip packages

With an effective resolution bandwidth of 18 GHz and a sample rate of 55 - 65 GSa/s the device is at the leading edge of converter performance. The device employs a self contained background calibration technique which improves the linearity of the internal transfer function. The calibration block also contains an alarm function which can be used as an interrupt to warn the system when any of the internal calibration DACs reaches a predefined or programmable percentage of its calibration range. From a system perspective it could be used as a warning of a possible problem caused by ageing or high temperature drift.

Luke Test Chip Features

The Luke test chips used with the evaluation platform each contain 2 channels of the 40nm CHAIS ADC. Each of these channels has RAM at its output which is used to store 16K X 8 bit samples from the ADC. The data can only be accessed by reading this memory as there is no direct external output from the ADC. Control/programming functions and RAM read operations are all done via an SPI interface.

There are several storage modes available which enable control of the RAMs from external triggers.

Main features of the Luke test chip is the same as for the ADC macro, with these additional items:

- 2 Channel version of the 40nm macro
- 2 x 16K samples memory space (1 per ADC)
- SPI Interface
- Output data: read from RAM via SPI
- Manufactured in high performance 1148 pin FCBGA

Development Kits

A development kit is available for the CHAIS ADC evaluation test chip (LUKE).

Each kit includes:

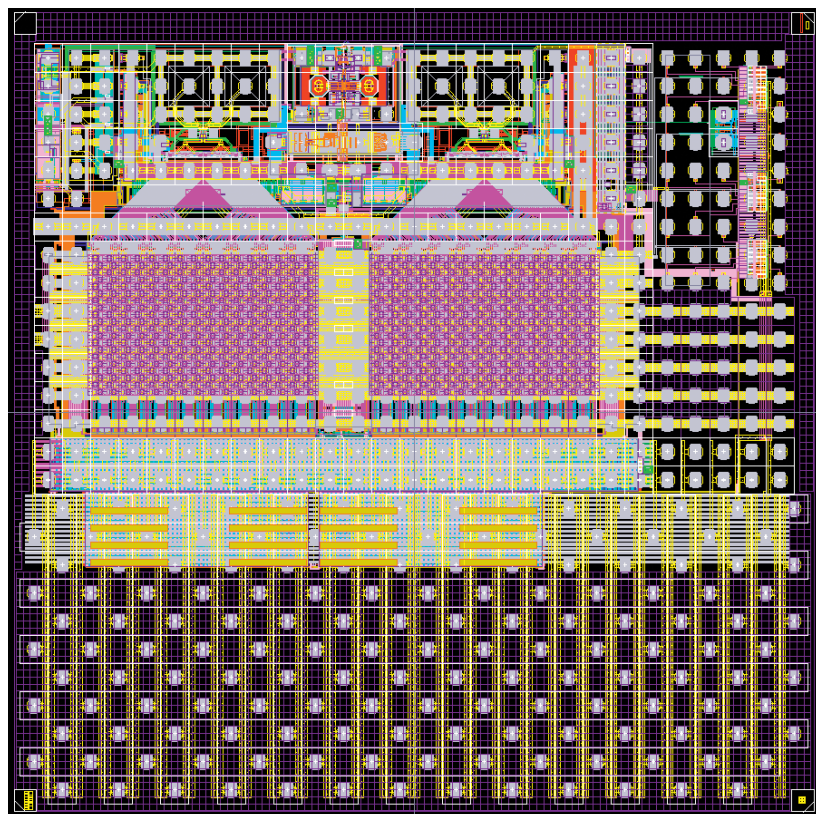
- Evaluation board with choice of LUKE being solder mounted or with socket for easy replacement
- Mains power supply and voltage regulator board
- Interconnect leads/boards
- Software

The kit includes everything needed to minimise the time taken to get started.

A USB interface is provided on the evaluation board for simple connection to a PC.

Part Numbers

- **LUKE-DK1** – This evaluation board is supplied with one LUKE-ES device mounted directly on to it
- **LUKE-DK2** – This evaluation board is supplied with two LUKE-ES devices mounted directly on to it
- **LUKE-DK-SOCKET1** – This evaluation board is supplied with one low inductance socket fitted. Test chips are sold separately (LUKE-ES)
- **LUKE-DK-SOCKET2** – This evaluation board is supplied with two low inductance sockets fitted. Test chips are sold separately (LUKE-ES)
- **LUKE-ES** – Luke ADC test chips



Plot of Luke 40nm CHAIS ADC

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