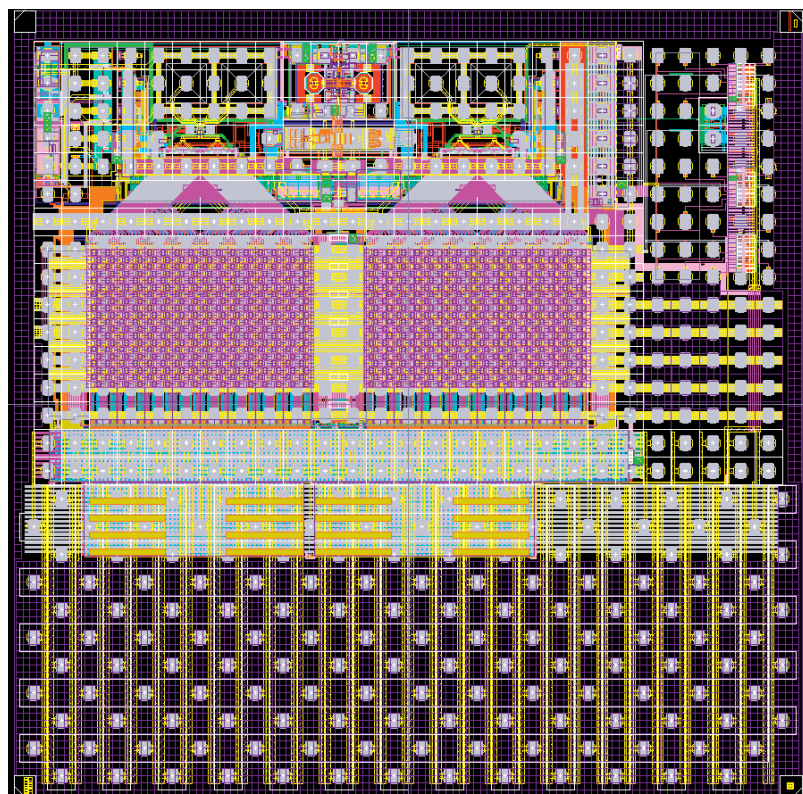


LUKE-ES

Analog to Digital Converter

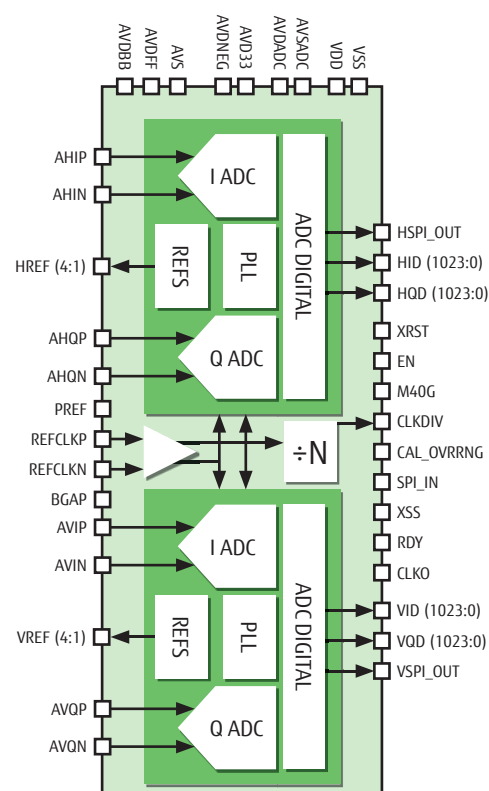


A Plot of the 40nm CHAIS ADC Test Chip (known as Luke)

Fujitsu's ultra fast CHAIS ADC has been responsible for the early enablement of real 100G transport networks. This is largely due to the extremely high sample rate of the ADC but also the IPs availability in CMOS technology which allows for a compact low power solution. The first generation of 100G optical receiver devices was based upon 65nm CMOS technology, but as we look toward the next step this technology must be ported to a more advanced process to enable greater functionality whilst staying within a stringent power budget.

The next step along the road map is the 40nm version of the CHAIS ADC macro. By moving to this process technology the designer can integrate more custom logic while maintaining or even reducing the device power consumption relative to a 65nm device. The CHAIS ADC macro power consumption scales by around

50% when moving from 65nm to 40nm but of course the big saving is to be had in the customer's digital circuit. This enables further enhancements over the first generation of 100G solutions. The customer should now be able to include the additional logic required to implement a soft decision FEC which effectively improves the sensitivity of the receiver by increasing its ability to recognise and correct incoming data. A further benefit in using the 40nm technology is that it would also be possible to integrate transmit functionality into the ASIC thus making a more compact solution. These integrated transmit functions can be further enhanced with the addition of a DAC to directly drive signals out to the optical modules. A suitable 40nm DAC capable of up to 65GSa/s (known as Leia) will be available to customers who wish to start their 40nm ASIC developments today.



Full ADC macro block diagram

ADC Macro Features

- Fujitsu 40nm Technology
- Resolution : 8-Bit
- 4 Channels (2 x IQ pairs)
- Sampling Rate : 55 – 65 GS/s
- Power Supply : 1.8V, 0.9V, -0.9V, -1.8V
- Power Consumption : 1.2W/ch
- DNL : ± 1 LSB, INL : ± 3.0 LSB
- ENOB: 5.7 (-6dBFS sinewave at ~8GHz)
- Differential Analog Input : 0.7VPPDiff
- 20GHz -3dB Input Bandwidth
- 2's Complement Data Format
- Output Rate: 128Samples @ 511.9MHz
- 0.9V Data Output Clock @ 511.9MHz
- REFCLK÷N programmable output clock
- 1.75 – 2GHz Input Reference Clock
- Internal 13.44 – 16.38GHz Differential VCO
- Self contained background calibration
- Calibration over-range flag
- Designed for flip-chip packages

Applications

- 40G/100G Communications Systems
- Test Equipment

Test Chip (Luke) Features

The Luke test chips used with the evaluation platform each contain 2 channels of the 40nm CHAIS ADC. Each of these channels has RAM at its output which is used to store 16K X 8 bit samples from the ADC. The data can only be accessed by reading this memory as there is no direct external output from the test chip. Control / programming functions and RAM read operations are all done via an SPI interface. There are several storage modes available which enable control of the RAMS from external triggers.

Main features of the Luke test chip are similar to the ADC macro, except for these differences:

- 2 Channel version of the 40nm macro
- 2 x 16K samples memory space (1 per ADC)
- SPI Interface
- Output data: read from RAM via SPI

Development Kits

A kit is available for the evaluation of the Luke test chip.

Each kit includes:

- Evaluation board with choice of LUKE being solder mounted or with socket for easy replacement
- Mains power supply and voltage regulator board
- Interconnect leads/boards
- Software

The kit includes everything needed to minimise the time taken to get started. A USB interface is provided on the evaluation board for easy connection to a PC.

Part Numbers

- **LUKE-DK1** – This evaluation board is supplied with one LUKE-ES device mounted directly on to it
- **LUKE-DK2** – This evaluation board is supplied with two LUKE-ES devices mounted directly on to it
- **LUKE-DK-SOCKET1** – This evaluation board is supplied with one low inductance socket fitted. Test chips are sold separately (LUKE-ES)
- **LUKE-DK-SOCKET2** – This evaluation board is supplied with two low inductance sockets fitted. Test chips are sold separately (LUKE-ES)
- **LUKE-ES** – Luke ADC test chips