Fujitsu Semiconductor Europe

Factsheet
100Gbps Coherent Demonstrator

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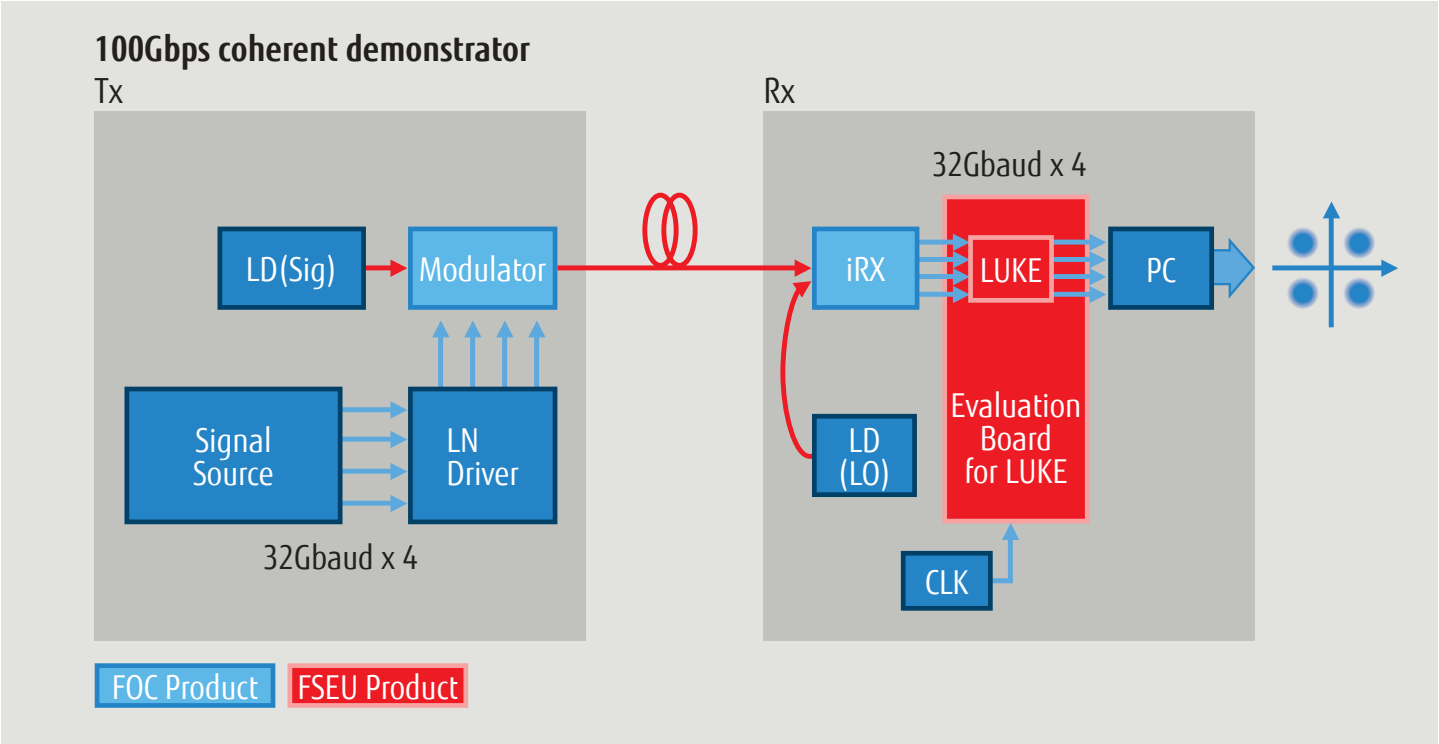


Functional diagram of Fujitsu 100G transmission

Demo Description

This Fujitsu 100G coherent demonstrator consists of an optical transmitter, a 100G DP-QPSK receiver evaluation board from Fujitsu Optical Components (FOC) and an ADC evaluation board, code named "Luke-DK", from Fujitsu Semiconductor Europe (FSEU).

The main characteristics of the 100G DP-QPSK low-case receiver module and ADC evaluation board are shown below.

100G Receiver Module

Key Features

- 128Gbps receiver module with DP-QPSK transmission format
- Exceptional dynamic performance balanced PIN/TIA photo receivers and 90 degree hybrid are integrated in one package
- Power consumption: 1.0W typ.
- OIF compliant
- RoHS compliant

Application

- 128Gbps DP-QPSK optical communication systems

Functional Description

- Based on OIF standards
- 8 photo-detectors, comprised of 4 sets of balanced detectors
- 4 linear amplifiers with differential outputs
- 2 ninety degree hybrid mixers with differential outputs
- Polarisation splitter to separate the input signal into two orthogonal polarisations, with each polarisation delivered to a hybrid mixer
- Polarisation maintaining power splitter, splitting the local oscillator power equally to two hybrid mixers
- Automatic Gain Control (AGC) and manual gain control
- User settable independent output level adjustment for each of the four outputs
- Peak indicator for each output
- DC blocker for each output
- All the above is in one hermetically sealed package

ADC Evaluation Board

The 40nm CHAIS (Charge-Mode Interleaved Sampler) ADC evaluation board is intended to allow system prototyping and evaluation for communication and measurement applications.

Key Features

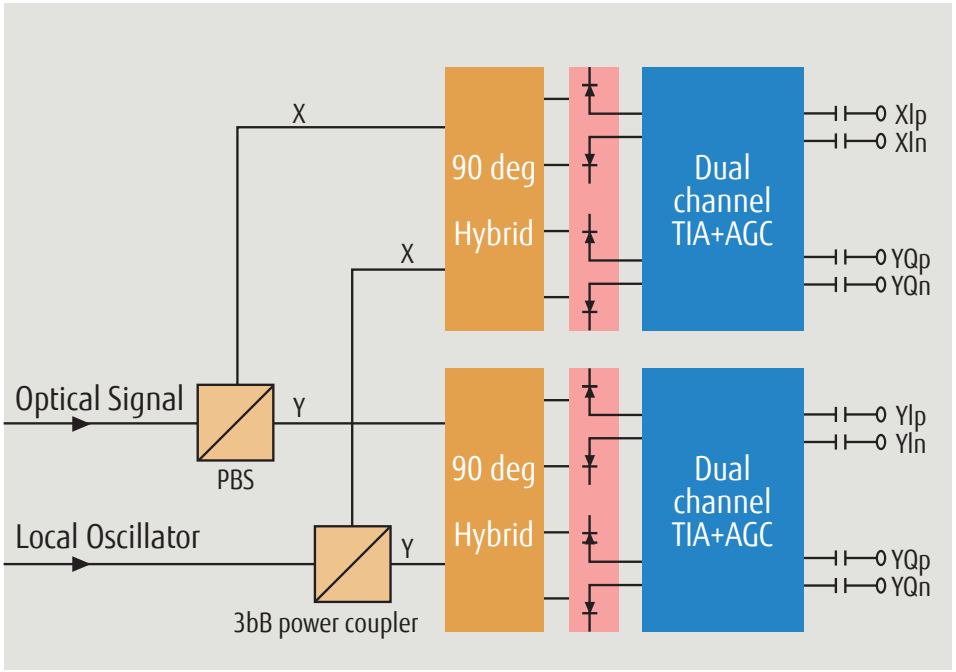
- 1 or 2 Luke test chips mounted to a high-performance printed circuit board giving up to 2×IQ pairs(4×55-65Gsps ADC)
- Low loss PCB materials providing superior signal integrity
- SMPM ADC input connectors
- Software for control of the device from host PC
- Integrated USB interface
- Clock distribution circuitry
- Dual device synchronisation
- 100-250V AC mains powered

Application(s)

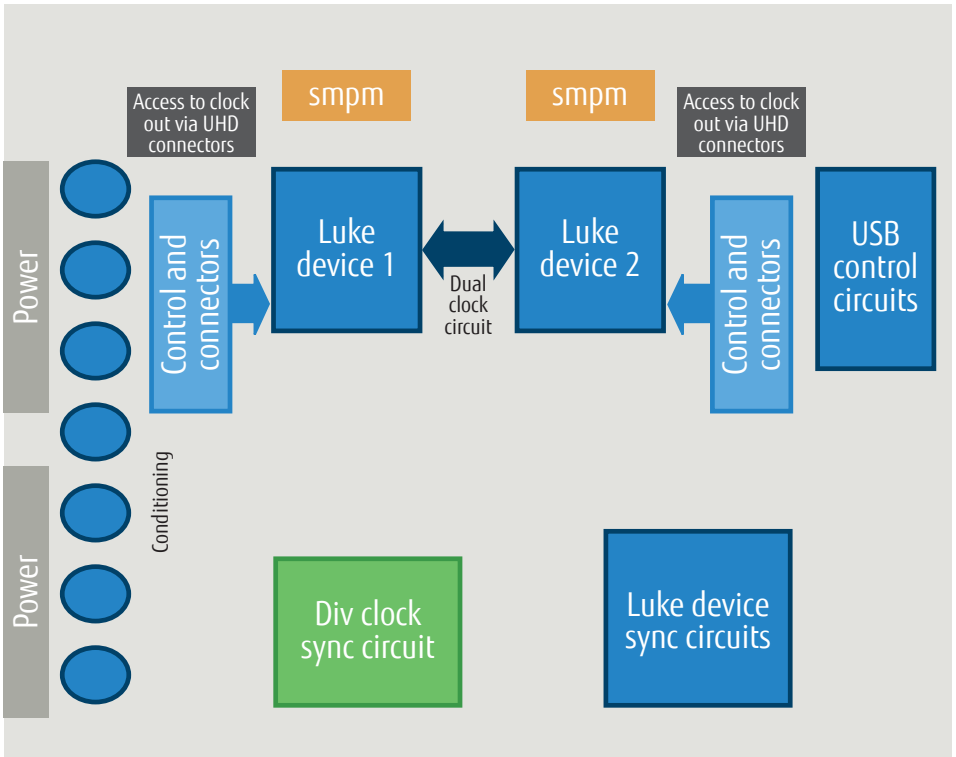
- 40G/100G Communications Systems
- Test Equipment

Functional Description

- The Luke test chips used with the evaluation platform each contain 2 channels of 40nm CHAIS ADC
- Each channel can store the digitizsed analogue input signal into on-ship RAM with 16K×8bit samples per ADC
- Data can only be accessed by reading memory as there is no real-time output from the ADC
- Control/Programming functions and RAM read operations via an SPI interface
- Several storage modes available which enable control of the RAMs from external triggers



Functional diagram of the 100G DP-QPSK receiver



Luke-DK ADC evaluation board

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