Fujitsu Semiconductor Europe

Factsheet
ASIC/COT CS86 Series

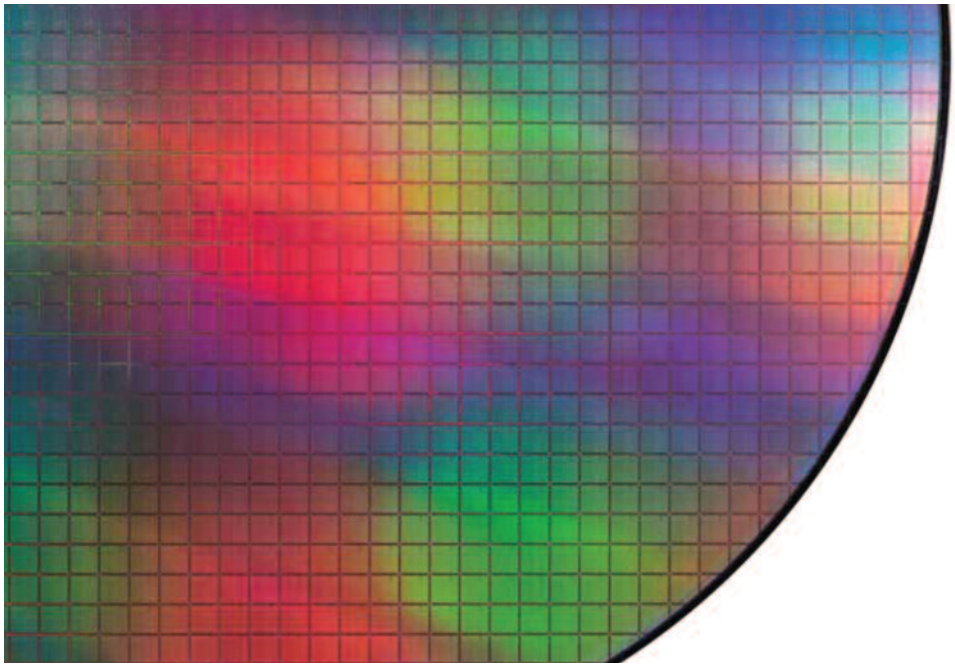
ASIC/COT - 180nm CMOS Technology CS86 Series

The CS86 series of 0.18µm standard cells is a line of CMOS ASICs based on higher integration implemented by introducing wiring pitch reduction technology and on I/O pad placement technology to the conventional 0.18µm series.

The CS86 series has three types of cell sets (CS86MN, CS86MZ, and CS86ML), covering a variety of applications,from portable devices requiring low power consumption to image processors requiring large-scale circuitry and high speed. The three types of cell sets can be contained on one chip, allowing those system LSIs to be implemented which require low power consumption as well as high-speed operation for certain types of processing.

Features

- Technology
  - 0.18µm silicon-gate CMOS, 5 to 6 layer wiring
  - Standard transistor cells can coexist with either ultra high-speed process cells or low leakage process cells on a chip
- Supply voltage : 1.8 V ± 0.15 V (standard) to 1.1 V ± 0.1 V
- Junction temperature range: −40 to +125°C
- Cell sets
  - CS86MN: Offers standard transistor characteristics. Designed as a library for products requiring higher throughputs
  - CS86MZ: Offers transistor characteristics for ultra high-speed operation. Designed as a library for products that require higher processing speeds than those provided by CS86MN
  - CS86ML: Offers transistor characteristics with less leak current. Designed as a library for mobile devices and other products requiring lower power consumption
- Output buffer cells with noise reduction circuits
- Input buffer cells and bidirectional buffer cells with on-chip input pull-up/pull-down resistors



200mm wafer

- Buffer cells for crystal oscillation circuits
- Special interfaces : SSTL2, PCI, P-CML, T-LVTTL, USB, IEEE1394, and others. Capable of incorporating compiled cells (RAM/ROM/Register file/Delay line)
- Configurable internal bus circuits
- Package lineup: QFP, LQFP, HQFP, FBGA

IP macro

CPUFR-V, ARM9, and others	
DSPCommunications DSP, DSP for Digital AV, and others	
Peripheral macro	Interval timer, interrupt controller, DMA controller, RTC, calender, UART, and others
Interface macro	PCI, IEEE1394, USB, IrDA, and others
Multimedia processing macros	JPEG, MPEG 4.0, and others
Mixed signal macros	ADC, DAC, OPAMP, and others
Compiled macros	RAM (1 port, 2 ports), ROM, Delay Line, Register file, and others
PLL	Analog PLL
I/O macro	Compatible with various interface levels between 1.1 V and 5 V; SSTL2, PCI, P-CML, T-LVTTL, USB, IEEE1394, and others

Note: ARM is the trademark of ARM Limited in the EU and other countries.

Design support and methodology

Fujitsu provides excellent local design centre support with front-end and back-end service. In addition, worldwide service organisations are available for global support.

Fujitsu's Reference Design Flow provides the following functions that help shorten the development time of large scale and high quality LSIs.

- High reliability design estimation in the early stage of physical design realised by physical prototyping
- Layout synthesis with optimised timing realised by physical synthesis tools
- High accuracy design environment considering drop in power supply voltage, signal noise, delay penalty and crosstalk
- I/O design environment (power line design, assignment and selection of I/Os, package selection) considering noise

Absolute maximum ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply voltage*1	V_{DD}	−0.5	+2.5*2	V
			+4.0*3	
Input voltage*1	V_I	−0.5	V_{DD} +0.5 (≤ 2.5V)*2	V
		−0.5	V_{DD} +0.5 (≤ 4.0V)*3	
Output voltage*1	V_O	−0.5	V_{DD} +0.5 (≤ 2.5V)*2	V
		−0.5	V_{DD} +0.5 (≤ 4.0V)*3	
Storage temperature	T_{STG}	−55	+125	℃
Junction temperature	T_J	−40	+125	℃

*1: V_{SS} = 0V *2: Internal gate area when single-power supply and dual-power supply are used. *3: I/O area when 3.3 V I/F or 2.5 V I/F is used with dual-power supply.

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