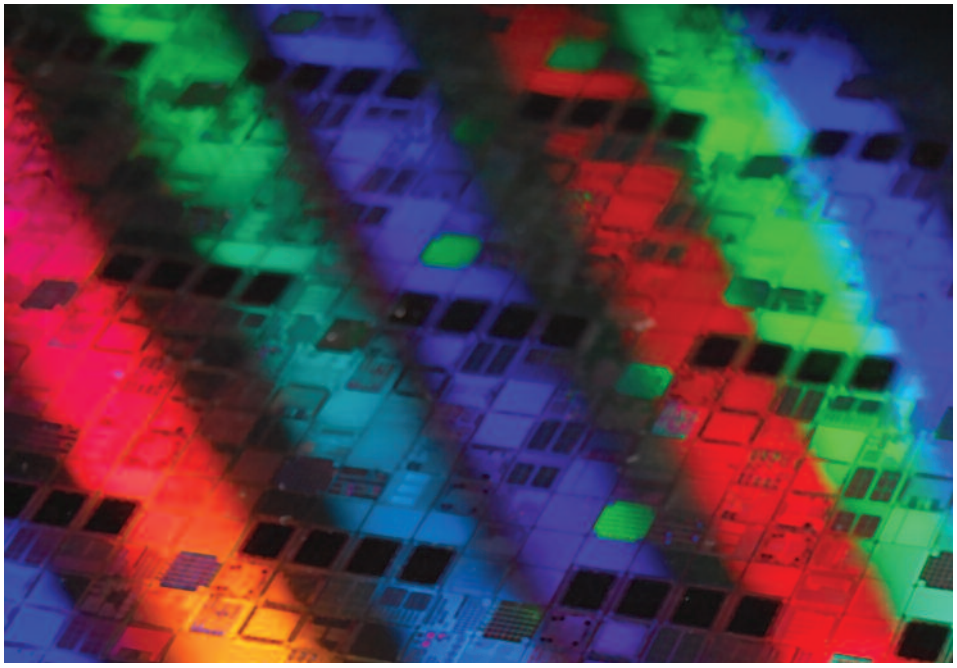
Fujitsu Semiconductor Europe

Factsheet
ASIC/COT CS302 Series

ASIC/COT - 40nm CMOS Technology CS302 Series

The CS302 series of 40 nm standard cells is a line of CMOS ASICs that satisfy demands for lower power consumption, higher speed and higher integration.

These cells offer the minimum level of leakage current in the semiconductor industry, and are able to implement a mixture of core transistors with three different threshold voltages, as appropriate for the applications ranging from handheld terminals to digital audio-visual equipment. The integration level in this series is twice that of the 65nm series with lower power consumption.



Features

- Technology
  - 40nm Si-gate CMOS
  - Maximum 11-metal layers. Extreme Low-K (ultra low permittivity) material is used for dielectric inter-layers
  - Three different types of core transistors (low leak, standard and high speed) can be used on the same chip
- Supply voltage: +1.1V ±0.1V
- Junction temperature range: -40 to +125°C
- Gate power consumption
  - 1.02nW / gate (operating condition 1.1V, operating rate 0.5, 1MHz)
- Supports various cell sets (from low power versions to high speed versions)
- It supports energy-saving mode, multi mode SRAM
- Compiled cells (RAM, ROM, others)
- Supports low-consumption technology
- Supports ultra high speed (up to 10Gbps) interface macros
- Special interfaces (LVDS, SSTL, others)
- Supports boundary SCAN test
- Supports use of industry-standard libraries
- Supports use of industry-standard tools
- Short-term development using a physical prototyping tool
- One pass design using a physical synthesis tool
- Hierarchical design environment for supporting large-scale circuits
- Supports Signal Integrity, EMI noise reduction
- Supports static timing sign-off
- Improve timing convergence by using Statistical Static Timing Analysis (SSTA)
- Design For Manufacturing (DFM) enables stable product-supply and reduced variation
- Package line-up: FBGA, PBGA, TEBGA, FC-BGA

Note: Including items under development

IP portfolio

Fujitsu offers an extensive IP line-up, including CPU cores (ARM®7 / 9 / 11 and Cortex™-A9 / R4 / M3 / M0 / M4 / A5 / A15), image cores, encryption, interface controllers, high-speed I/Os and mixed signal macros, all prepared for 40nm ASIC/COT.

Compiled cell

Compiled cells are macro cells that can be automatically generated by specifying the bit/word configuration. A big portfolio of compiled cells is available for the CS302 series (note that the bit/word ranges for each macro vary depending on the column type).

Special I/O interface macro

Special I/O	LVDS, SSTL2, SSTL18, PCI, I^2C
Interface macro	USB2.0 Device/host, Serial-ATA, PCI-Express, DDR2/3, HDMI, others

Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{DD}	−0.4	+1.5	V	*2
		−0.5	+2.5		*3
		−0.5	+3.6		*4
		−0.5	+4.6		*5
Input voltage*1	VI	−0.5	V_{DD} +0.5 (≤ 2.5V)	V	*3
		−0.5	V_{DD} +0.5 (≤ 3.6V)		*4
		−0.5	V_{DD} +0.5 (≤ 4.6V)		*5
Output voltage*1	VO	−0.5	V_{DD} +0.5 (≤ 2.5V)	V	*3
		−0.5	V_{DD} +0.5 (≤ 3.6V)		*4
		−0.5	V_{DD} +0.5 (≤ 4.6V)		*5
Storage temperature	T_{STG}	−55	+125	℃	
Operation junction temperature	Tj	−40	+125	℃	
Output current*6	IO	–	–	mA	
Power supply pin current*7	ID	–	–	mA	

*1: V_{SS} = 0V, *2: Internal gates, *3: 1.8V interface on dual-power supply system, *4: 2.5V interface on dual-power supply system, *5: 3.3V interface on dual-power supply system, *6: The output current varies depending on the number of wiring layers in the chip and the wiring configuration of the I/O cells, *7: The power supply pin current depends on the type of chip frame.

Electrical characteristics

Parameter	Symbol	Conditions	Value			Unit
			Min	Type	Max	
'H' level input voltage	V_{OH}	–	2.4	–	V_{DDE}	V
'L' level input voltage	V_{OL}	–	0	–	0.4	V
'H' level output current	I_{OH}	2mA cell @V_{OH} (Min)	−13.2	−7.8	−3.9	mA
		4mA cell @V_{OH} (Min)	−26.3	−15.6	-7.9	
		8mA cell @V_{OH} (Min)	−52.7	−31.2	−15.8	
		12mA cell @V_{OH} (Min)	−79.0	−46.8	−23.7	
		16mA cell @V_{OH} (Min)	−105.1	−62.3	−31.5	
		24mA cell @V_{OH} (Min)	−140.0	−82.9	−42.0	
'L' level output current	I_{OL}	2mA cell @V_{OL} (Max)	2.2	3.5	4.8	mA
		4mA cell @V_{OL} (Max)	4.4	7.0	9.5	
		8mA cell @V_{OL} (Max)	8.9	13.9	19.1	
		12mA cell @V_{OL} (Max)	13.3	20.9	28.6	
		16mA cell @V_{OL} (Max)	17.8	27.9	38.1	
		24mA cell @V_{OL} (Max)	26.6	41.8	57.2	
Input leakage current	IL	–	−10	–	+10	µA
Pull-up resistor	Rpu	VI = 0V	29	41	62	kΩ
Pull-down resistor	Rpd	VI = V_{DDE}	30	44	72	kΩ

- DC Characteristics (Dual power supply: V_{DDE} = 3.3V, V_{DDI} = 1.1V) (preliminary values) Measurement conditions: V_{DD} = 3.3 ±0.3V, V_{DDI} = 1.1V ±0.1V, V_{SS} = 0V, Tj = −40 to +125°C
- DC Characteristics (Dual power supply: V_{DDE} = 1.8V, V_{DDI} = 1.1V)
- DC Characteristics (Dual power supply: V_{DDE} = 2.5V, V_{DDI} = 1.1V)

Design methods

Fujitsu Semiconductor's Reference Design Flow provides the following functions that help reduce the development time of large scale, high quality LSIs.

- Statistical Static Timing Analysis (SSTA) improves timing convergence
- Physical Prototyping enables more accurate estimation of highly reliable designs
- Layout synthesis with optimised timing is realised by Physical Synthesis Tool
- High accuracy design environment considers drop in power supply voltage, signal noise, delay penalty and crosstalk
- I/O design environment (power line design, assignment and selection of I/Os, package selection) considers noise

Packages

The CS302 series can use the same packages that were available for the previous series, allowing a smooth transition from previously developed models. For details of delivery times, contact Fujitsu Semiconductor Europe.

- FBGA packages
- PBGA packages
- TEBGA packages
- FC-BGA packages

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