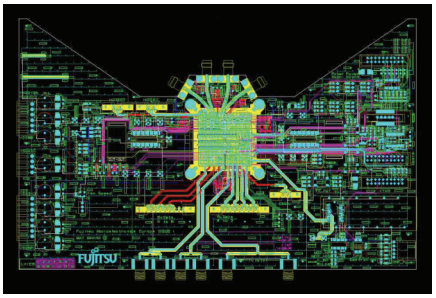
FACTSHEET
56GSa/s 8-BIT ADC DEVELOPMENT KIT

FUJITSU

56GSa/s 8-bit ADC development kit



ADC evaluation board allows early silicon characterisation of Fujitsu's CHAIS ADC technology

Description of evaluation board

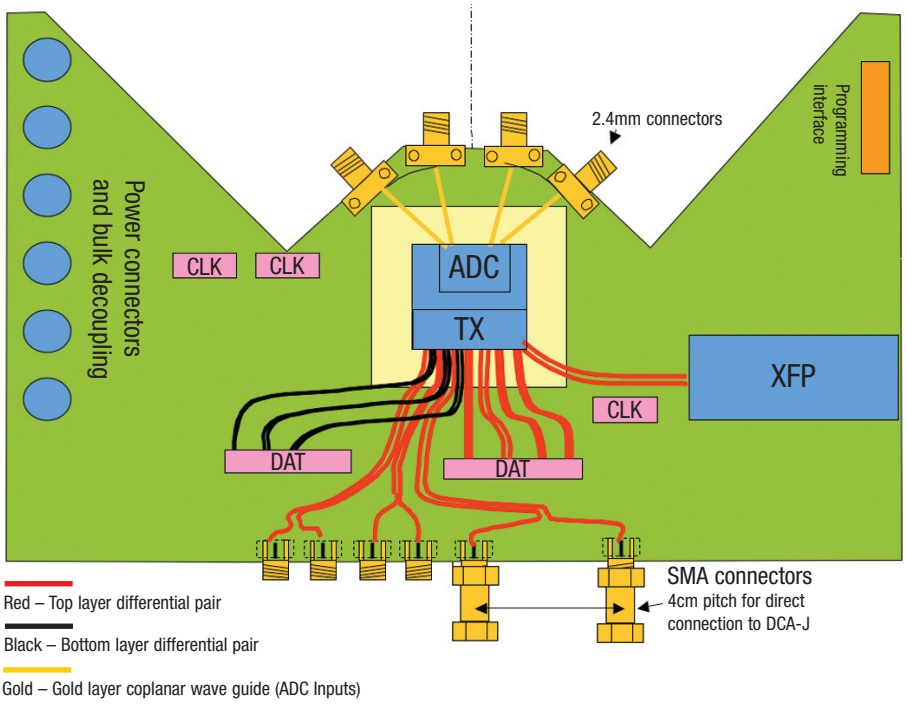
The 56 GSa/s ADC evaluation board (BATBOARD) allows early silicon characterisation of Fujitsu's CHAIS (CHArge-mode Interleaved Sampler) ADC technology, and provides very fast data capture for high-speed signals. With two channels of 56GSa/s 8-bit ADCs packaged in a single ROBIN device, it provides unique features to simplify measurement and evaluation in the lab. It is ideal for prototyping next generation test and measurement systems as well as trials towards new communication technologies.

Two variants of the board are available. Version 1 has a device soldered down for maximum performance. Version 2 uses a low inductance socket which allows replacement of the device under test, with a small reduction in performance. Special attention has been given to the connector choice to allow connection to instrumentation that will perform the design verification tests. The board uses low-loss RF material to optimise the integrity of the signals.

Each kit includes:

- BATBOARD evaluation board with choice of ROBIN being soldered or socketed
- Calibration board
- High frequency splitter board
- Interconnect boards
- PC programming interface board
- Software

The kit includes everything needed to minimise the time to get started, including evaluation board, PC-USB interface and PC software utility.



Features

- Device mounted on a high performance PCB
- Superior signal integrity from low loss materials
- 2 delay matched 56GSa/s ADC
- On-chip memory to store captured input signals
- 2.4mm ADC input connectors specified to 50GHz
- Software for control of the device from host PC
- Option to mount a low inductance socket to allow replacement of device under test

Applications

- Fast data sampling for lab purposes
- Evaluation and characterisation of Fujitsu CHAIS ADC technology
- Prototyping of leading-edge measurement systems or optical front ends.

DK Part Numbers

- BATBOARD-DK: This evaluation board is supplied with a soldered ADC chip
- BATBOARD-DK-SOCKET: This evaluation board is supplied with a low inductance socket.

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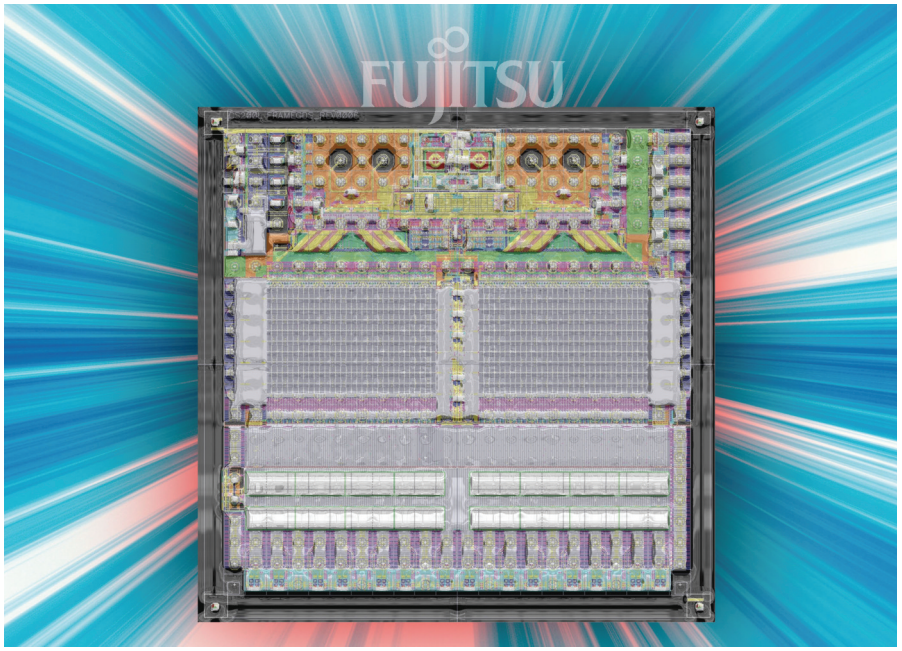


CHAIS technology enables integration of extremely fast ADCs in CMOS process technology

Description of CMOS ADC

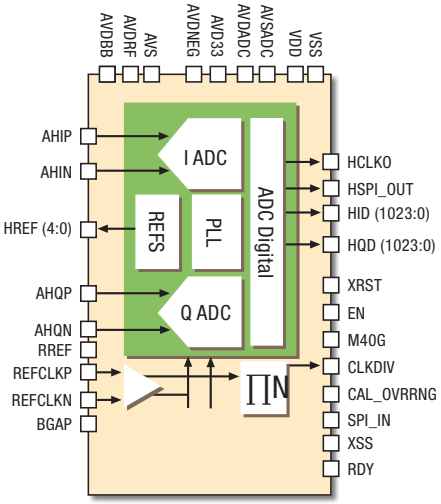
Fujitsu's ultra-fast CMOS ADC enables upcoming telecommunication applications, such as 100G Ethernet and OTU-4 transport systems using coherent receivers. The ADC uses Fujitsu's revolutionary CHarge-mode Interleaved Sampler technology (CHAIS), which allows the implementation of extremely fast and high resolution ADCs in CMOS process technology.

Major benefits of the CHAIS ADC are low power consumption and the possibility to be integrated with millions of gates onto the same die using Fujitsu's standard 65nm CMOS process technology. In combination with Fujitsu's leading flip-chip packaging technology, the ultra-fast ADC is ideal for applications that require high performance analogue and huge digital processing power while maintaining a reliable and proven manufacturing flow.

ADC Target Applications

- Test equipment
- Fast data conversion
- Optical communications systems

ADC block diagram



Block diagram and pin functionality of the 8-bit ADC

Features

- Fujitsu 65nm CMOS process technology
- Resolution: 8-bit
- Sampling rate: 56GSa/s
- Power supply: -1.2V, 1.2V, 3.3V
- Power consumption: 2W per channel (typical)
- DNL: ±0.5 LSB, INL : ±1.0 LSB
- SNDR: 40dBFS @Fin=1GHz, 36dBFS @Fin=17GHz
- Differential analogue Input: $1.0V_{PPD}$
- >15GHz -3dB input bandwidth
- Two's complement data format
- Output rate: 128 samples x 8-bit @437.5MHz
- 1.75GHz input reference clock
- Internal 14GHz VCO/PLL per I/Q ADC pair
- 56GSa/s ADCs configured as two I/Q Pairs
- <100fs rms jitter
- <500fs I/Q sample time error
- Continuous background calibration for sampler interleave timing skew as well as linearity and offset
- Calibration warning and over-range flags
- Designed for flip-chip

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