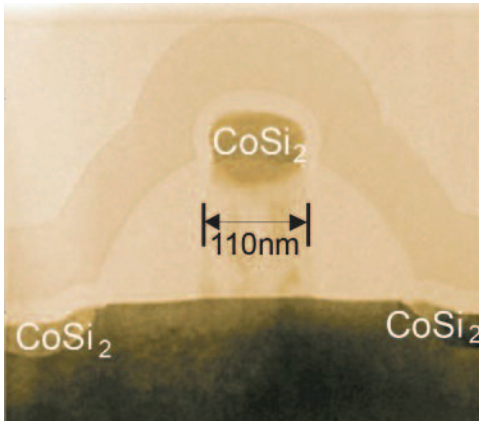


ASIC/COT - 110nm CMOS technology CS91 series



110nm transistor

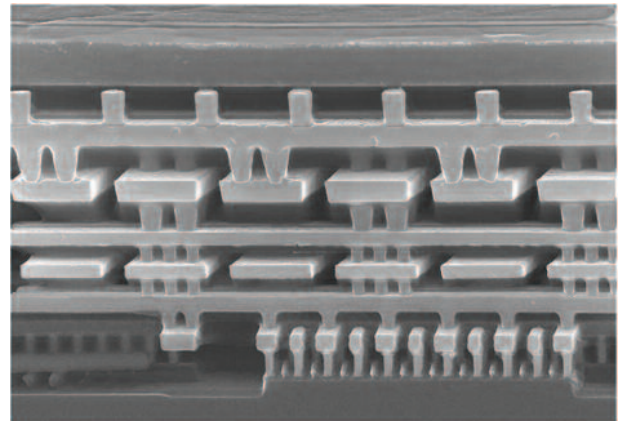
Description

Fujitsu's CS91, a 110nm standard-cell product, is based on Fujitsu's state-of-the-art CMOS process technology, a deep sub-micron process designed for today's high-speed and low-power SoC products. The cell library, which is optimised for synthesis-based designs, has accurate timing and power-characterised data, cell areas, and statistical wire-load models. The CS91 standard-cell library contains both high-performance and high-density cells, giving designers the option of combining both types of standard cell blocks on the same chip. The CS91 library supports popular third-party tools and data-exchange file standards. The CS91 chip cores can operate at 0.8 to 1.3V range. The I/Os, operating at 0.8 to 3.6V range, can conveniently interface with various types of devices. Interface options include low-swing, high-speed I/Os and high-speed bus interface I/Os.

Also provided in CS91 are high performance and area-optimised memories, mixed-signal blocks, analogue functions, a rich set of IP Cores and Mega Macros, and various I/O interfaces.

IP Portfolio

- Networking & Communication
POS- PHY level 3 & level 4, OC3 & OC12 Sonet Framer Utopia I/II, 10/100 MAC
- Processors
ARM7, ARM9 & ARM11
- Standard bus controllers & bus bridges
USB(1.1) device/host controller, USB(2.0) PHY PCI-X, PCI (2.1) - 33MHz, 66MHz & PCI host controller 1394 Link & PHY - 400 Mbps
- Multimedia access & wireless
JPEG, MPEG, Video encoder
- Memory controllers
ARM Cache, FCRAM™, SDRAM, DDR controller
- ARM & other peripherals
Various ARM peripherals DMA Controller (8 Ch), UART, interrupt controller, I²C



CS91, ILD: Silk, CU-7 layers

Packages for 0.11µm ASIC products

Fujitsu's advanced flip chip BGA packages are specially designed for high-speed back plane applications using 2.5 to 3.125G I/Os. Besides FCBGA packages, Fujitsu's advanced packaging also offers traditional QFP and Heat-spreader QFP packages, TAB-BGA, enhanced BGA (EBGA) and fine-pitch BGA (FBGA) packages in various pin/ball pitch and in a wide range of pin-counts.

FACTSHEET

ASIC/COT CS91 SERIES

Design support and methodology

Fujitsu's design methodology ensures first-time silicon success by integrating proprietary point tools with popular, sign-off-quality CAD tools such as:

- Automatic I/O frame generator & packaging rule checker
- Test insertion, ATPG
- Memory compiler
- Logic & test design rule checker
- Power analysis & optimisation
- High-precision library characterisation & delay calculator

Fujitsu's clock-driven design methodology is devised for low power and low skew. The methodology identifies the best-suited clock distribution strategy for a given design and predicts performance in advance. Fujitsu supports co-simulation, emulation and high-level floor planning to optimise the power, timing, and size of the design. This enables the designer to make effective architectural-level decisions to achieve optimal design solutions. Fujitsu's design-for-test strategy includes boundary scan (JTAG) and full and partial scan, as well as a built-in self-test for both logic and memory.

Features

Technology

- 110nm channel length
- Low resistive Cu interconnect for high performance
- Low-k dielectric to reduce parasitic capacitance

Cell Library

- Four cell libraries to provide design flexibility and trade-off between ultra high performance and low standby power

- Very high density: 200k raw gates/mm²
- High-density diffused RAMs and ROMs
- High-speed mixed-signal macros
- Analogue PLLs

CS91 standard cells in four various library types

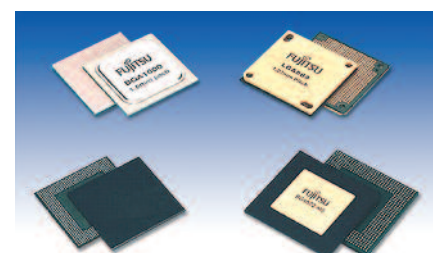
- CS91HU (ultra high speed transistor) for applications requiring ultra high performance
- CS91HZ (high speed transistor) for applications requiring high performance at low power
- CS91HN (normal transistor) for applications requiring high performance with low leakage
- CS91SN (normal transistor) for high density with low-power applications

High Speed & Standard I/Os

- 2.5 to 3.125G I/Os
- OIF & XAUI standards
- Standard I/Os: LVTTTL, SSTL, HSTL, LVDS, P-CML

Application specific IPs

- Controller cores: ARM cache, FCRAM controller
- Connectivity cores: USB, PCI, I²C, Ethernet, IEEE1394



Example: High pin count BGA packages

Wide variety of packaging

- Flip chip BGA: 450 to 2,116 pins, designed for high-speed I/Os
- Enhanced BGA, TAB BGA, fine pitch BGA, plastic BGA, QFP & HQFP

CS91 maximum ratings

Parameter		Symbol	Maximum Ratings	Unit
Power Supply Voltage	1.2V (typ.)	V _{DD}	-0.5 to +1.35	V
	2.5V (typ.)	V _{DD}	-0.5 to +3.6	
	3.3V (typ.)	V _{DD}	-0.5 to +4.6	
Input voltage		V _I	-0.5 to V _{DD} +0.5	V
Storage temperature	Plastic	T _{ST}	-55 to +125	°C
	Ceramic	T _{ST}	-65 to +125	
Junction temperature		T _J	-40 to +125	°C

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