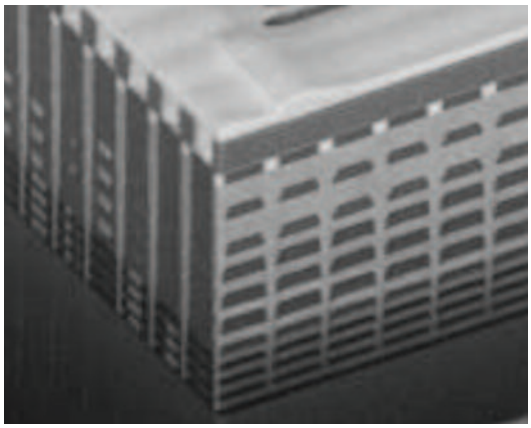
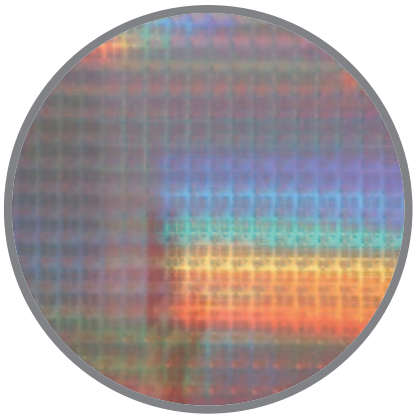
FACTSHEET
ASIC/COT CS101 SERIES

FUJITSU

ASIC/COT - 90nm CMOS technology CS101 series



Very low-k dielectric 9 Cu/1Al interconnect



300mm wafer

Features

- High integration
  - Transistor of 80nm gate length (ITRS road map 90nm)
  - 10 layer fine pitch, copper wiring, and low-k insulatingmaterial techniques
  - Maximum 91 million gates (nearly twice that of 0.11µm technology)
- Low power consumption/low leakage current
- I/O with pad structure with fine pad pitch technology for chip size reduction
- High-speed library and low-power library available
  - High-speed: CS101HZ, CS101MZ, CS101SZ
  - Standard: CS101HN, CS101MN, CS101SN
  - Low leak: CS101SL
- Small gate propagation delay, tpd = 12ps (@1.2V, inverter, and F/O=1)
- Compiled memory macros (SRAMs, ROM and others)
- Application-specific IPs
  - Computational cores: ARM, DSPs for communication and digital-AV
  - Mixed signals: ADCs and DACs
  - HSIF logics: PCI-Express
- High-speed interface SerDes macros (~10Gbps data rate)
  - Standard I/Os: LVTTL, SSTL, HSTL, LVDS. P-CML
- Wide supply voltage (0.90V or 1.30V for core)
- Various packages available (QFP, FBGA, EBGA, PBGA, FC-BGA)

Description

CS101 series, a 90nm standard cell product, is a CMOS ASIC that satisfies users' demands for lower power consumption and higher speed. The leakage current of the transistors is the minimum level in the industry. Three types of core transistors with a different threshold voltage can be mixed according to user application. The design rules match industry standards, and a wide range of IP macros are available for use.

IP portfolio

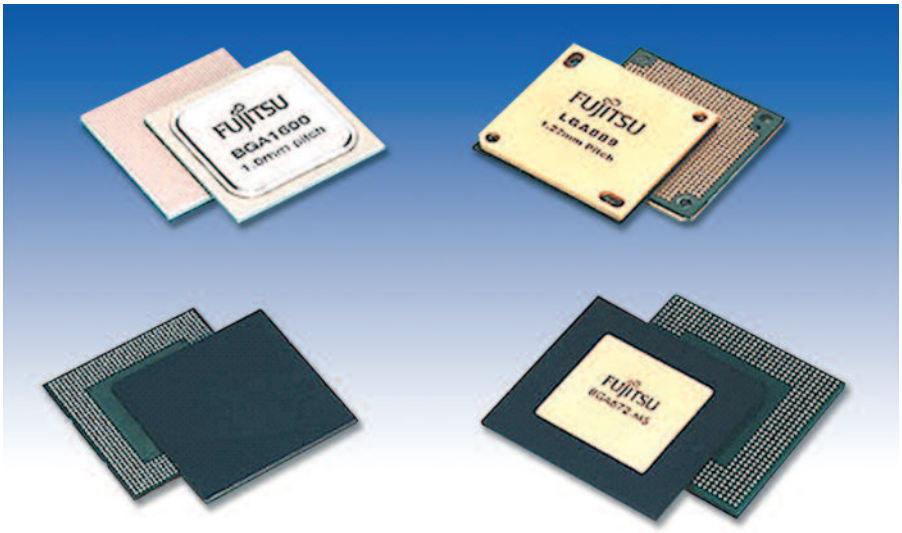
Fujitsu offers an extensive IP line-up, including CPU cores, image cores, encryption, interface controllers and high-speed IOs, all prepared for 90nm ASIC/COT.

Design support and methodology

Fujitsu provides excellent local design centre support with front-end and back-end service. In addition, worldwide service organisations are available for global support.

Fujitsu's Reference Design Flow provides the following functions that help shorten the development time of largescale and high quality LSIs.

- High reliability design estimation in the early stage of physical design realised by physical prototyping.
- Layout synthesis with optimised timing realised by physical synthesis tools.
- High accuracy design environment considering drop in power supply voltage, signal noise, delay penalty, and crosstalk.
- I/O design environment (power line design, assignment and selection of I/Os, package selection) considering noise.



Example: High pin count BGA packages

CS101 Maximum ratings

Parameter	Symbol	Maximum Ratings	Unit	Note
Power Supply Voltage	V_{DDI}	-0.5 to 1.8	V	For internal logic
	V_{DDE}	-0.5 to 3.6	V	For 2.5V external I/Os
		-0.5 to 4.6	V	For 3.3V external I/Os
Input Voltage	V_I	-0.5 to VDDI+0.5	V	For internal logic
		-0.5 to VDDE+0.5	V	For 2.5V and 3.3V external I/Os
Output Voltage	V_O	-0.5 to VDDI+0.5	V	For internal logic
		-0.5 to VDDE+0.5	V	For 2.5V and 3.3 external I/Os
Storage Temperature	T_{STG}	-55 to +125	°C	For plastic packages
Junction Temperature	T_J	-40 to +125	°C	

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Contact us on +49(0) 61 03 69 00 or visit
http://emea.fujitsu.com/microelectronics