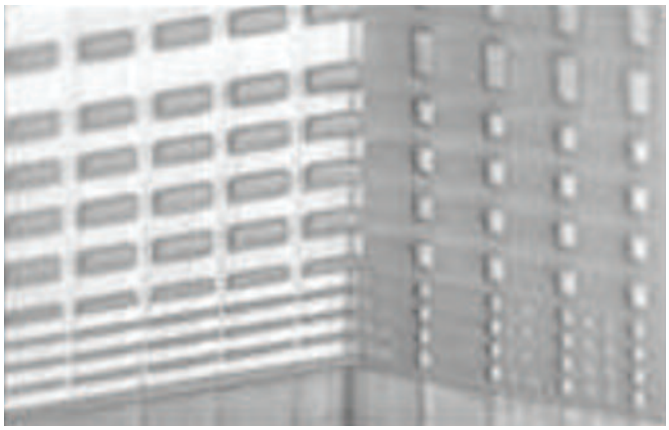
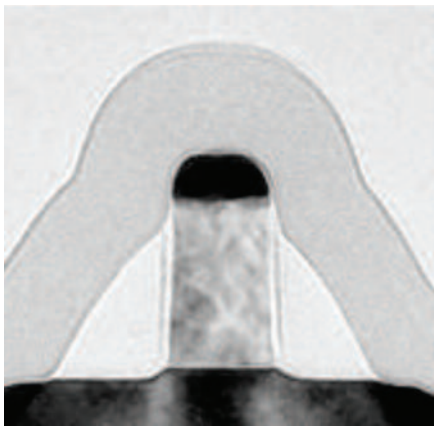
FACTSHEET
ASIC/COT CS202 SERIES

FUJITSU

ASIC/COT - 65nm CMOS technology CS202 series



11Cu/1Al interconnect



50nm gate length

Features

- Transistor of 50nm gate length
- 12 layer fine pitch, copper wiring, ultra low-k (low permittivity) insulating material techniques
- 3 different types of core transistors: ultra low power, low power, high speed useable on the same chip
- Low power consumption/low leakage current
- I/O with pad structure with fine pad pitch technology for chip size reduction
- Compiled memory macros (SRAMs, ROM, others) 1T-SRAM-Q® (MoSys Inc.)®
- Application-specific IPs
  - Computational cores: ARM, DSP for communication and digital-AV
  - Mixed signals: ADCs and DACs
- High-speed interface: PCI-Express, SATA, SerDes, FPD link
- I/Os: LVTTL, SSTL2/18, mobile-DDR, LVDS, USB, others
- Supply voltage (internal) 1.0V ± 0.1V to 1.2V ± 0.1V
- Various packages available (QFP, FBGA, EBGA, PBGA, FC-BGA)

Description

The CS202 series of 65nm standard cells is a line of CMOS ASICs that satisfy demands for lower power consumption and higher integration. These cells offer the minimum level of leakage current in the semiconductor industry, and are able to implement a mixture of core transistors with three different threshold voltages, as appropriate for applications ranging from hand-held terminals to digital audio/visual equipment.

The integration level in this series is twice the previous series with lower power consumption.

IP portfolio

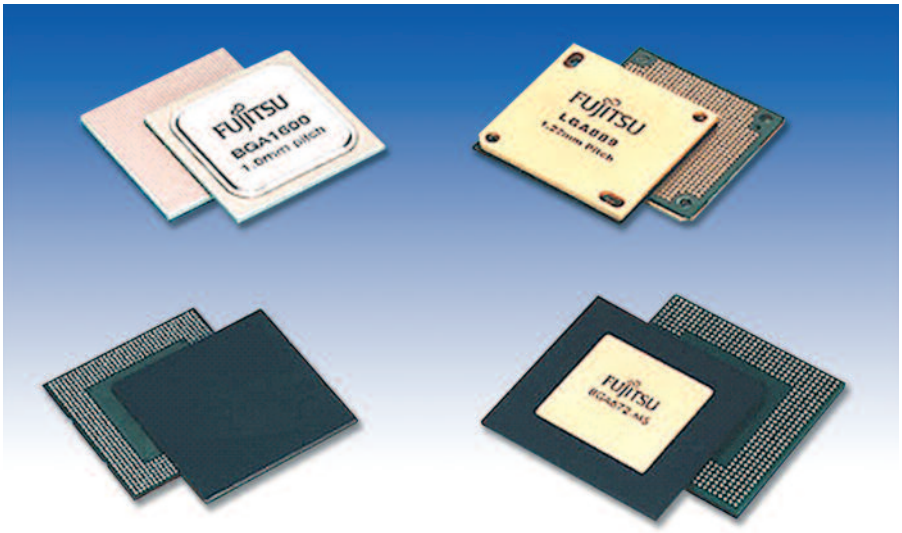
Fujitsu offers an extensive IP line-up, including CPU cores (ARM7, ARM9, ARM11), image cores, encryption, interface controllers, high-speed IOs and mixed signal macros, all prepared for 65nm ASIC/COT.

Design support and methodology

Fujitsu provides excellent local design centre support with front-end and back-end service. In addition, worldwide service organisations are available for global support.

Fujitsu's Reference Design Flow provides the following functions that help reduce the development time of large scale, high quality LSIs.

- Statistical Static Timing Analysis (SSTA) improves timing convergence
- Physical prototyping enables more accurate estimation of highly reliable designs
- Layout synthesis with optimised timing is realised by physical synthesis tool
- High accuracy design environment considers drop in power supply voltage, signal noise, delay penalty and crosstalk
- I/O design environment (power line design, assignment and selection of I/Os, package selection) considers noise



Example: High pin count BGA packages

CS202 maximum ratings

Parameter	Symbol	Maximum Ratings	Unit	Note
Power Supply Voltage	V_{DD}	-0.5 to 1.8	V	For internal logic
		-0.5 to 2.5	V	For 1.8V external I/Os
		-0.5 to 3.6	V	For 2.5V external I/Os
		-0.5 to 4.6	V	For 3.5V external I/Os
Input Voltage	V_I	-0.5 to V_{DD}+0.5 (≤2.5V)	V	For 1.8V external I/Os
		-0.5 to V_{DD}+0.5 (≤3.6V)	V	For 2.5V external I/Os
		-0.5 to V_{DD}+0.5 (≤4.6V)	V	For 3.3V external I/Os
Output Voltage	V_O	-0.5 to V_{DD}+0.5 (≤2.5V)	V	For 1.8V external I/Os
		-0.5 to V_{DD}+0.5 (≤3.6V)	V	For 2.5V external I/Os
		-0.5 to V_{DD}+0.5 (≤3.6V)	V	For 3.3V external I/Os
Storage Temperature	T_{ST}	-55 to +125	°C	
Junction Temperature	T_J	-40 to +125	°C	