

New development platform & evaluation board for **EMBEDDED ARM-BASED ASICs**



The T-Engine board features the MB87Q1100 platform chip, developed in 0.11 μ m technology, which contains the two ARM cores, the ARM946ES and ARM926EJ-S, both running at 200MHz.

Fujitsu's T-Engine board features a two-arm-core chip

Fujitsu's new development platform and evaluation board allows customers to produce embedded ARM-based ASICs.

Containing a specially developed Fujitsu platform chip featuring two ARM cores, this is the first ARM-related development platform to be launched by Fujitsu.

It is based on the T-Engine, an open hardware and software standard for real-time development that has been produced by the T-Engine Forum. This group was established by the TRON project, a consortium of many global electronic companies, to create a standardised development environment for controllers in embedded applications.

Key board features

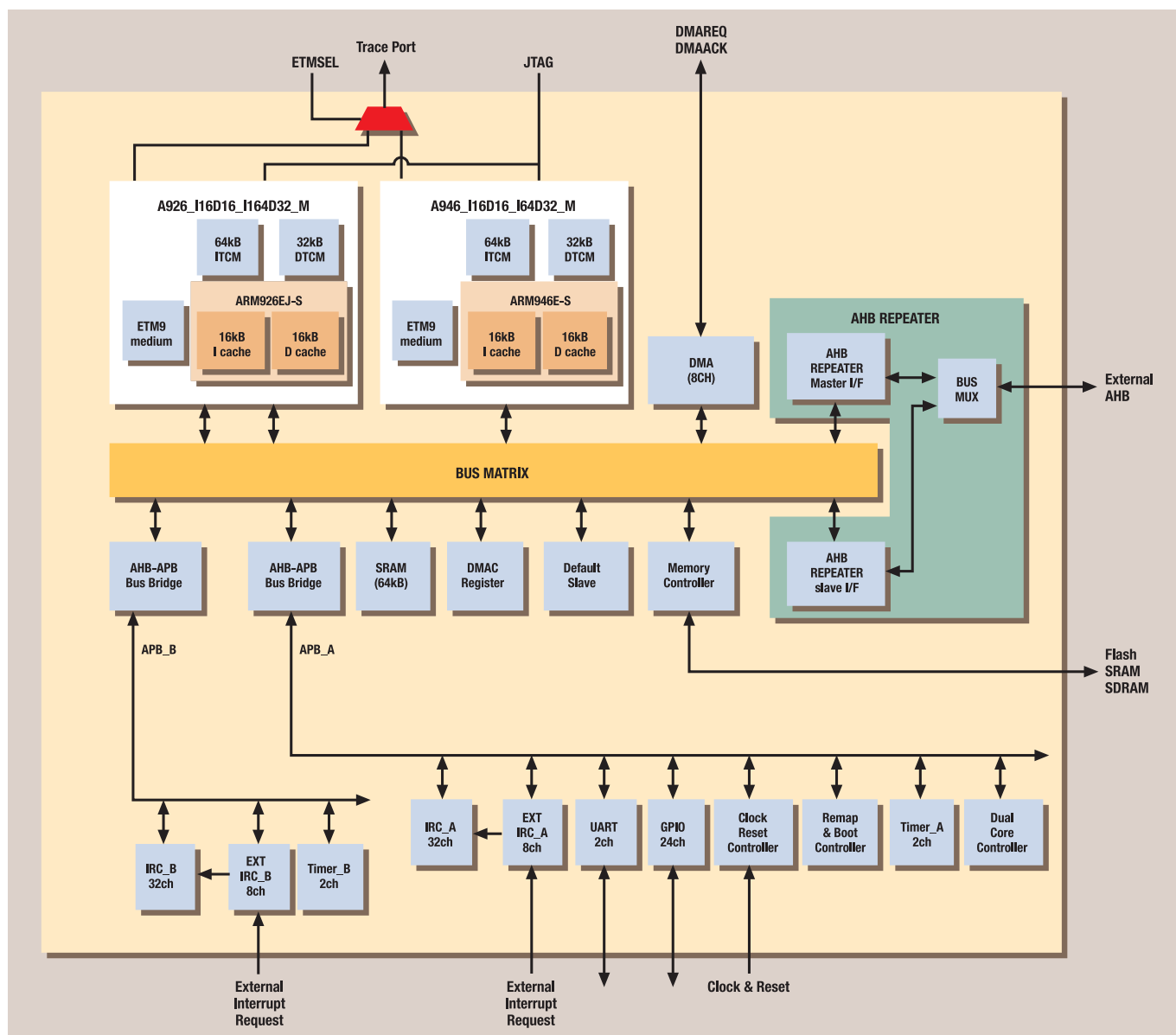
Fujitsu's new T-Engine board features its MB87Q1100 platform chip, developed in 0.11 μ m technology, which contains the two ARM cores, the ARM946ES and ARM926EJ-S, both running at 200MHz. Users can run each core in single mode, or if greater performance is required, in dual mode, giving a throughput of about 400MIPS.

Key chip features

Other features of the new platform chip include: multi-layer AHB architecture (five layers), realising high performance and low power consumption; each core with its own interrupt controller; clock generator with embedded PLL macro; memory controller that supports SRAM, SDRAM and Flash; 64kB internal RAM on AHB; 8-channel DMA, UART and 24 GPIOs implemented; and dual core controller.



This T-Engine board (shown at actual size 120x75mm) contains Dual ARM9 platform chip MB87Q1100 and therefore offers a powerful SoC development platform.



The architecture of the dual ARM core makes it possible to achieve overall performance of more than 400MIPS in dual-core mode.

Development & evaluation

The T-Engine board functions as both a software development environment, and also as an evaluation board with the capacity to build system hardware. In order to do this, customers will need an additional FPGA board that implements the necessary peripheral blocks.

The standard T-Engine specification

This calls for an extremely small CPU board size, measuring only 75 x 120mm. It specifies a 32-bit CPU, 16- or 32MB of RAM and 4MB of flash memory. Other features of the standard are: serial I/O of 384kbps (or more possible); one PCMCIA II slot; and USB host – type A connector, one channel.

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