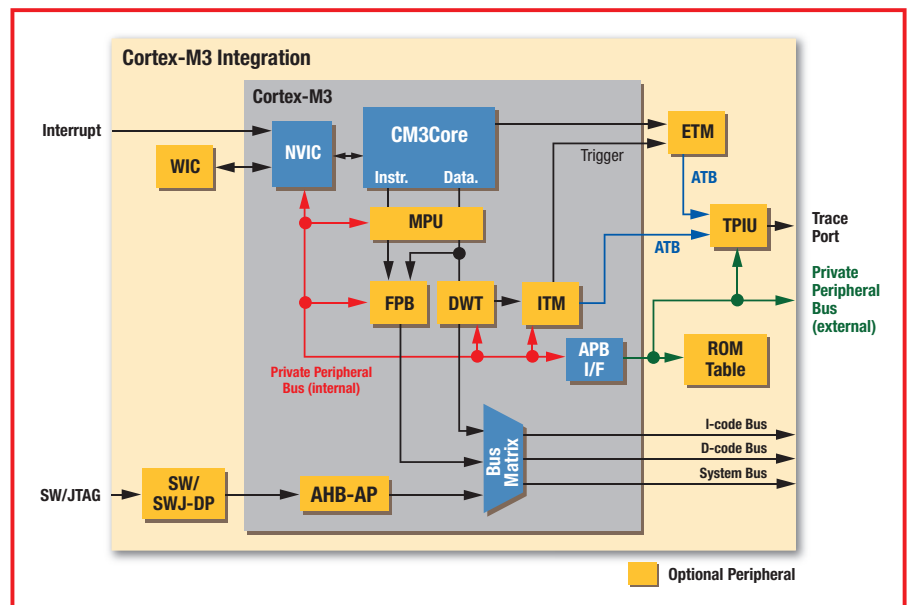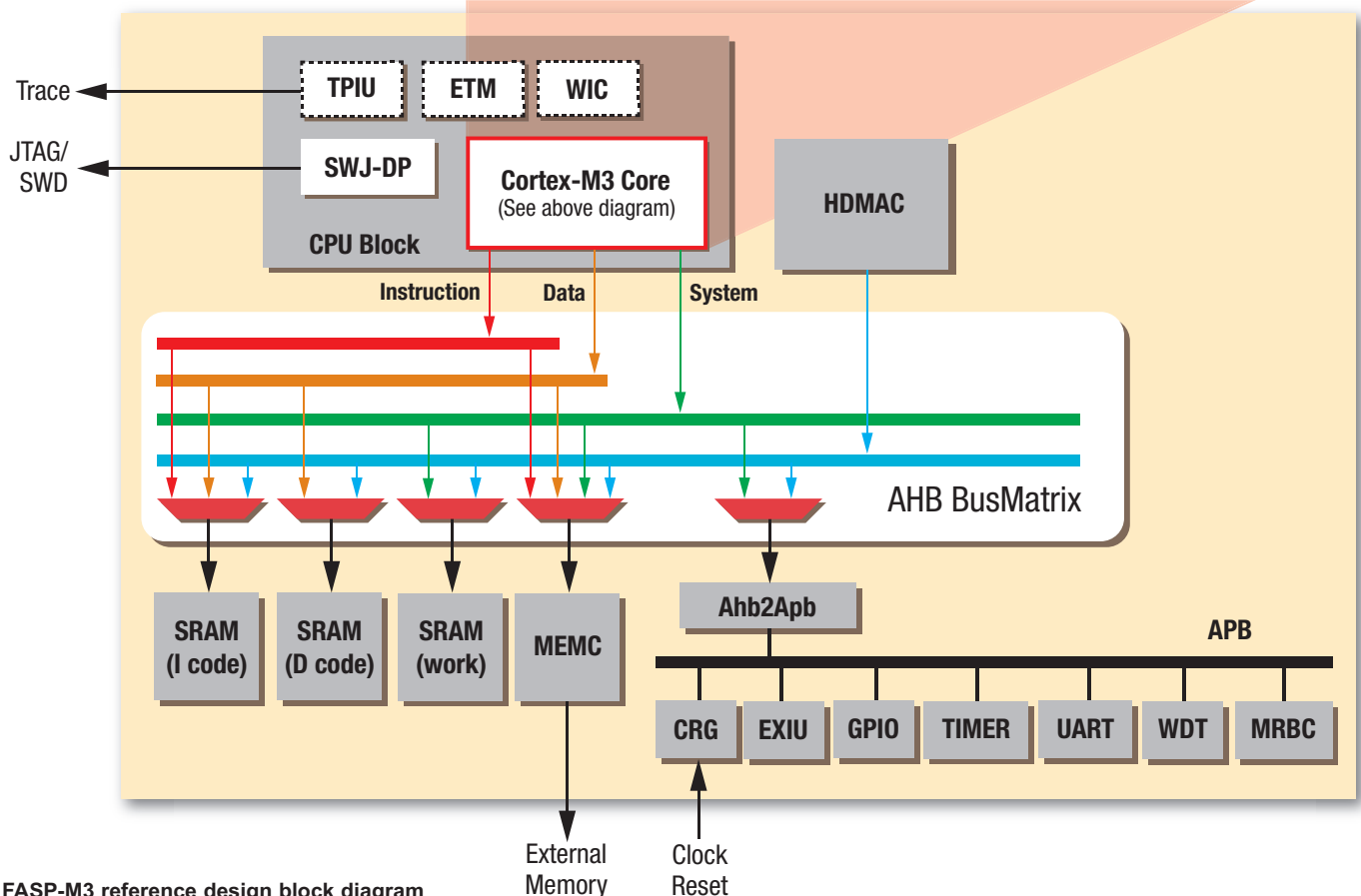FUJITSU

FASP-M3 reference design concept

Fujitsu's reference design concept has the ARM® Cortex-M3™ 32-bit processor at its heart, which was specifically developed to provide a high-performance, low-cost platform for many applications including microcontrollers, automotive body systems, industrial control systems and wireless networking.

The Cortex-M3 processor provides outstanding computational performance and exceptional system response to interrupts while meeting low cost requirements through small core footprint, industry-leading code density enabling smaller memories, reduced pin count and low power consumption.

Detailed view of the Cortex-M3 Core

FASP-M3 reference design block diagram

FASP-M3 concepts

- Base platform
  - Only basic peripherals are implemented
- Easy customisation, easy chip development
  - By changing the configuration of Cortex-M3
  - By adding or removing peripherals, replace BusMatrix
  - By changing interrupt signal assignment

Features

- 32-bit high-performance and low-cost processor
- ARMv7-M architecture, 3-stage pipeline, Harvard architecture
- 1.25DMIPS/MHz
- Thumb®-2 instruction set provides enhanced levels of performance, energy efficiency, and code density
- Reduced pin count for lower packaging costs
- Substantial debug features
  - Serial Wire Debug implements debug with just 2 pins
  - Single Wire Viewer implements single pin trace profiling
- Configurable (Many optional components)
  - MPU, FPB, DWT, ITM, ETM, WIC, SWJ/SW-DP
  - Trade-off between the size and functionalities
- Interrupt
  - NVIC (Nested Vectored Interrupt Controller) enables low latency interrupt handling - Configurable number of interrupt (default value max 240)
  - Configurable interrupt priority levels (max 256 level supported)
  - 16 external interrupts

- Bus Architecture
  - Multi-layer AHB (ADK™ 3.0 BusMatrix)
  - Use of Sparse Connect to reduce the bus confliction
  - AHB - APB bridge for slow peripherals
- Memory System
  - Internal SRAM
  - No wait access
  - Separate dedicated memory for instruction and data to obtain the best performance of Cortex-M3
  - Work SRAM shared by Cortex-M3 and other masters
  - 128kB for instruction, 32kB for data, 32kB for work by default. (valiable from 4kB to 1MB)
- SDRAM Interface
  - Support SDR SDRAM (max 128MB)
- External ROM SRAM Interface
  - Support NOR and NAND flash
  - 8 chip selects. Access timing is programmable
  - Address and data bus are shared with SDRAM I/F for Lower cost product
- Endian
  - Little Endian

- Low power modes
  - Sleep mode
  - Deep sleep mode
  - Stop mode

Deliverables for customers

- DSM of Cortex-M3 and ETM
  - For NC-Verilog on 64-bit Linux
  - For Modelsim on 64-bit Linux
  - For VCS on 32-bit Linux
- Reference Design of SoC (encrypted RTL)
- Simulation environment (Testbench, Simulation script)
- Boot code (initialisation of Cortex-M3 and peripherals)
- Documents (Specifications, User Guide, Implementation Guide)
- RTL simulation model
- Netlist simulation model
- Timing model
- Documents
  - Technical Reference Manual issued from ARM (open access)
  - Specification of Reference Design
  - Specifications of each Fujitsu's IP
  - FASP-M3 User's Guide

ARM

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