SPARC64™ XII:
Fujitsu’s latest 12 Core Processor
for Mission Critical Servers

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Agenda

◆ Fujitsu Processor Development History

◆ SPARC64™ XII
  ▪ Design concept
  ▪ Chip overview
  ▪ Micro Architecture
  ▪ System Architecture
  ▪ Performance

◆ Summary
Fujitsu Processor development

Perpetual evolution

Virtual Machine Architecture
Software on Chip
High-speed Interconnect

HPC-ACE
System on Chip
Hardware Barrier
Multi-core Multi-thread
L2$ on Die
Non-Blocking $
O-O-O Execution
Super-Scalar
Single-chip CPU
Store Ahead
Branch History
Prefetch

Mainframe/UNIX/HPC incremental development

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SPARC64™ XII Design Concept

High Performance: SPEED and THROUGHPUT

◆ High SPEED (Single thread performance)
  - High CPU frequency
  - State of the art O-O-O
  - Rich execution units

◆ High THROUGHPUT
  - Many cores, threads
  - Strong Cache and Memory

◆ Robust RAS
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  ■ Performance

◆ Summary
SPARC64™ XII Chip Overview

- **Architecture Features**
  - 12 cores x 8 threads
  - SWoC (Software on Chip)
  - 32MB L3 cache
  - Embedded Memory and IO Controller (PCIe GEN3)

- **20nm CMOS**
  - 25.8mm x 30.8mm
  - 5,450M transistors
  - 1,860 signal pins
  - 4.25GHz (up to 4.35GHz with High Speed Mode enabled)

- **Performance (peak)**
  - 417GIPS / 835GFlops
  - 153GB/s memory throughput
## SPARC64™ XII Core spec

<table>
<thead>
<tr>
<th>Instruction Set Architecture</th>
<th>SPARC-V9/JPS HPC-ACE VM / SWoC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integer Execution Units</td>
<td>(156 GPR x 4 + 96 GUB) x 2pipe</td>
</tr>
<tr>
<td></td>
<td>(ALU/SHIFT x2) x 2pipe</td>
</tr>
<tr>
<td></td>
<td>(ALU/AGEN x2) x 2pipe</td>
</tr>
<tr>
<td></td>
<td>(MULT/DIVIDE x1) x 2pipe</td>
</tr>
<tr>
<td>FP Execution Units</td>
<td>(128 FPR x 4 + 64 FUB) x 2pipe</td>
</tr>
<tr>
<td></td>
<td>(FMA x4 / FDIV x2) x 2pipe</td>
</tr>
<tr>
<td></td>
<td>(IMA/Logic x4) x2pipe</td>
</tr>
<tr>
<td></td>
<td>(Decimal x1 / Cypher x2) x 2pipe</td>
</tr>
<tr>
<td>L1$</td>
<td>L1I$  64KB/4way</td>
</tr>
<tr>
<td></td>
<td>L1D$  32KB/4way x 2pipe</td>
</tr>
<tr>
<td>L2$</td>
<td>512KB/16way</td>
</tr>
</tbody>
</table>
SPARC64™ XII Pipeline

Fetch | Decode | Issue | Reg-Read | Execute | Memory Access | Commit

Branch Prediction

L1 Instruction Cache 64KB

Instruction Buffer Decode

RSBR Reservation Station for Branch

RSA Reservation Station for Address generation

RSE Reservation Station for Execution

RSF Reservation Station for Floating-point

Branch Prediction

GPR x4

EAGA

EAGB

EXA

EXB

FPR x4

FLA

FLB

FLC

FPR Update Buffer

FUB

GUB

FLD

Store Buffer

L1 Data Cache 32KB
dTLB

Commit Stack Entry

Program Counter x4

Control Registers x4

Pipeline-0

Pipeline-1

12 cores

Enhanced in SPARC64™ XII

SPARC64™ XII

CPU-CPU i/f

MAC

IOC
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- Summary
Common Micro-Architecture features between SPARC64™ X+ and XII

◆ Processor Core
  ■ Fetch 8 instructions, Decode 4 instructions, Execute 6 instructions per instruction pipeline
  ■ Aggressive O-O-O execution, including memory access (load and store)
  ■ High single thread performance
  ■ SWoC (Software on Chip)
    Accelerates specific software function by hardware

◆ Outside the Core
  ■ Embedded Memory and IO Controller (PCIe GEN3)
  ■ Robust RAS (Reliability, Availability, Serviceability) ★
Reliability, Availability, Serviceability

<table>
<thead>
<tr>
<th>Units</th>
<th>Error detection and correction scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache (Tag)</td>
<td>ECC Duplicate &amp; Parity</td>
</tr>
<tr>
<td>Cache (Data)</td>
<td>ECC Parity</td>
</tr>
<tr>
<td>Register</td>
<td>ECC (INT/FP) Parity (Others)</td>
</tr>
<tr>
<td>Execution Unit</td>
<td>Parity/Residue</td>
</tr>
<tr>
<td>Cache dynamic degradation</td>
<td>Yes</td>
</tr>
<tr>
<td>HW Instruction Retry</td>
<td>Yes</td>
</tr>
<tr>
<td>History</td>
<td>Yes</td>
</tr>
</tbody>
</table>

→ Guarantees Data Integrity
(Number of checkers increased to ~66,000)

Green: 1bit error Correctable
Yellow: 1bit error Detectable
Gray: 1bit error harmless
Hardware Instruction Retry

1. Error
2. Flush
3. Single step execution
4. Update of SW visible resources
5. Back to normal execution after the re-executed Instruction gets committed without an error.

- When an error is detected, Hardware re-execute the instruction automatically to remove the transient error by itself.
Enhanced Micro-Architecture from SPARC64™ X+

◆ Processor Core
  ▪ Dual instruction pipelines sharing L1 I-cache, and 8-way SMT (4-way SMT per instruction pipeline) ★
  ▪ Better Branch Prediction Scheme
  ▪ Various Queue-size increase
  ▪ Deeper pipeline to increase Frequency
  ▪ High Speed Mode

◆ Outside the core
  ▪ 3 level hierarchy cache, and 4 LCU (Last level cache and Core Unit) structure ★
  ▪ DDR4-2400 memory
  ▪ Doubled PCIe GEN3 ports (8 lane x 4)
Micro-architecture enhancements 1/2

Increase core throughput, keep single thread performance

- Dual instruction pipelines per core
  - Each pipeline has its own resources except ↓

- Sharing L1 I-Cache and TLB between the two pipelines
  - Especially effective in DB apps

- 4-way SMT instruction pipeline
  - More throughput compared with the previous 2-way SMT
  - Resources are dynamically shared between the threads.

Core Resource allocation

<table>
<thead>
<tr>
<th>#Active threads</th>
<th>L1 I$</th>
<th>IB</th>
<th>Rsv. Station</th>
<th>Rename Registers</th>
<th>Execution Units</th>
<th>FP/SP Port</th>
<th>L1 D$</th>
<th>CSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100%</td>
<td>50%</td>
<td>50%</td>
<td>50%</td>
<td>50%</td>
<td>50%</td>
<td>50%</td>
<td>50%</td>
</tr>
<tr>
<td>2</td>
<td>100%</td>
<td>50% x2</td>
<td>50% x2</td>
<td>50% x2</td>
<td>100%</td>
<td>50% x2</td>
<td>100%</td>
<td>50% x2</td>
</tr>
<tr>
<td>4</td>
<td>100%</td>
<td>25% x4</td>
<td>25% x4</td>
<td>25% x4</td>
<td>100%</td>
<td>25% x4</td>
<td>100%</td>
<td>25% x4</td>
</tr>
<tr>
<td>8</td>
<td>100%</td>
<td>12.5% x8</td>
<td>50% x2</td>
<td>12.5% x8</td>
<td>100%</td>
<td>12.5% x8</td>
<td>100%</td>
<td>12.5% x8</td>
</tr>
</tbody>
</table>
Micro-architecture enhancements 2/2

3 level cache and 4 LCU structure to realize Low Latency and High throughput

- L2 cache latency < L3 cache latency x 0.5
- L2 cache to Core: 32 Bytes x 2 pipelines
- L3 cache to Core: 32 Bytes x 3 cores

- **MEZASI**
  - Fujitsu’s unique cache protocol for LCU
- **ELC (Extra Level Cache)**
  - Unused L3 cache blocks act as Victim Cache
- **IO-DCA (IO Direct Cache Access)**
  - Direct DMA write to L3 cache from IO device
- **Speculative memory access**
  - Memory access in parallel with other L3 cache blocks access
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Fujitsu SPARC M12 server

Fujitsu’s latest UNIX server with SPARC64™ XII.

- M12-2: mid-range server
- M12-2S: scalable high-end server
### SPARC M12 System Architecture

- Scales from 1 to 32 CPU sockets (2,048 → 3,072 threads)
  - Directory-based cache coherency
  - High-speed interconnect, up to 25 Gbps per lane in SPARC64™ XII

### System Configuration
- Building Block (BB) is 2 CPUs and 2 XBs
- Up to 4 BBs can be connected by XBs
- 16 BBs can be connected via XB-Boxes
- BB topology inherits current M10-4S with SPARC64™ X+

#### Building Block (2 CPU Sockets)

<table>
<thead>
<tr>
<th>CPU</th>
<th>XB</th>
</tr>
</thead>
</table>

- To other XBs ~168GBps (IN/OUT)

#### 16 BBs (32 CPU Sockets)

- 16 BBs can be connected via XB-Boxes
- Each BB has 2 CPUs and 2 XBs
- BBs are connected via XB-Boxes

- 25Gbps
- 14.5/14Gbps

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**Diagram:**

- BB#00 to BB#01
- BB#02 to BB#03
- BB#04 to BB#05
- BB#06 to BB#07
- BB#08 to BB#09
- BB#10 to BB#11
- BB#12 to BB#13
- BB#14 to BB#15
- BB#00 to XB-Box#0
- BB#01 to XB-Box#2
- BB#02 to XB-Box#1
- BB#03 to XB-Box#2
- BB#04 to XB-Box#1
- BB#05 to XB-Box#2
- BB#06 to XB-Box#1
- BB#07 to XB-Box#2
- BB#08 to XB-Box#1
- BB#09 to XB-Box#2
- BB#10 to XB-Box#1
- BB#11 to XB-Box#2
- BB#12 to XB-Box#1
- BB#13 to XB-Box#2
- BB#14 to XB-Box#1
- BB#15 to XB-Box#2

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SPARC M12 System Cooling

◆ VLLC (Vapor and Liquid Loop Cooling)
Newly developed cooling mechanism for SPARC M12.
- Evaporative cooling, taking heat away when liquid changes to vapor
- The pumps circulate coolant in the VLLC system
- The radiator dissipates the heat absorbed by the cooling plate into the air.

➔ Achieves 2x cooling performance of the current LLC
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<table>
<thead>
<tr>
<th>Benchmark</th>
<th>1CPU</th>
<th>2CPU</th>
<th>16CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECint®_rate2006</td>
<td>956</td>
<td>1,910</td>
<td>14,500</td>
</tr>
<tr>
<td>SPECjbb®2015 Composite</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max</td>
<td>52,659 jOPS</td>
<td>98,333 jOPS</td>
<td>n/a</td>
</tr>
<tr>
<td>Critical</td>
<td>34,771 jOPS</td>
<td>63,354 jOPS</td>
<td>n/a</td>
</tr>
<tr>
<td>SPECjbb®2015 Multiple-JVM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max</td>
<td>54,434 jOPS</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Critical</td>
<td>34,771 jOPS</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>STREAMtriad</td>
<td>127GB/s</td>
<td>n/a</td>
<td>1,533GB/s</td>
</tr>
</tbody>
</table>

Source except STREAMtriad: www.spec.org

Fujitsu SPARC M12-2S:
- SPARC64 XII (4.25GHz, up to 4.35GHz) x 1,2,16CPU
- OS: Oracle Solaris 11.3
- Compiler: Oracle Developer Studio 12.6
- JVM: HotSpot™ 64-Bit Server VM, version 1.8.0_121
**SPARC64™ XII Performance**

- **2x chip throughput and 2.5x core throughput** compared to previous SPARC64™ XII, keeping single thread performance
- **Keys:** 8way SMT design, Higher CPU frequency, and micro-architecture improvement

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**SPARC64™ XII relative performance (SPARC64™ X+ = 100%)**

- **2.3x-2.9x core throughput**
- **1.8x-2.2x chip throughput**
- **>1.0x single thread performance**
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◆ SPARC64™ XII is Fujitsu's 12th SPARC processor which has been designed to be used for Fujitsu's latest UNIX server.

◆ The processor enhancements are to increase throughput, while keeping its high single thread performance and its robust RAS features.

◆ SPARC64™ XII measured results have shown 2x chip throughput of SPARC64™ X+

◆ Fujitsu will continue to develop SPARC64™ series to meet the needs of a new era.