# Silicon Photonics Optical Transceiver for High-speed, High-density and Low-power LSI Interconnect

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**The next-generation servers and supercomputers with high performance and low power consumption require not only CPUs with an enhanced processing capability, but also signal transmission technology that connects CPUs with other CPUs or memories at high density and low power. It is becoming difficult for electrical signal transmission to satisfy the demand for the next-generation servers and supercomputers due to the decrease of transmission distance in high-speed transmission and the restriction of the numbers of pins. Therefore, there have been increasing expectations for optical interconnects enabling large-capacity (wide bandwidth) and long-distance transmission. Thus, there are high hopes that it will be a key technology. Especially, silicon (Si) photonic interconnects have been attracting much attention in recent years because they are considered to be promising for reducing the size, increasing integration density and lowering the power consumption of optical transceivers. This paper explains Fujitsu's and Fujitsu Laboratories' small, energy-efficient Si photonics optical transceiver technologies. The key factors for realizing a small, high-density optical transceiver with low power consumption involve enhancing optical devices and driver circuits, and optimizing the mounting structure to supply high-quality power and signals. We proposed a novel configuration for a Si photonic transceiver utilizing a bridge structure that enabled high-density integration without wiring, and we optimized the design of optical/electrical devices based on this structure. We achieved the world's best performance in terms of high signal density and low power consumption, and demonstrated the effectiveness of the technology.**

## 1. Introduction

High-end servers and next-generation supercomputers support cloud computing and super-large-scale computing today. To meet the increasing demands placed on data processing to cater to these computers, CPUs are evolving to increase their processing capability by enhancing the performance with advances in the semiconductor process technology, and adopting multiple-core CPUs. To realize a high-performance system, it is necessary not only to enhance the CPU capacity, but also to increase the bandwidth for signal transmission that connects the CPU with other CPUs, memories and other external devices. With conventional copper-wiring-based signal transmission, it is becoming difficult to meet the ever-increasing demands for signal transmission; faster transmission results in a shorter transmission distance, higher power consumption, and the number of pins for interconnects is limited. Optical transmission—an optical interconnect—is seen as technology capable of overcoming these obstacles in electrical signal transmission.

Currently, board-edge and on-board types of optical interconnects, as shown in **Figure 1 (a)** and **(b)**, are being developed and marketed. However, these optical interconnects have the following problems:

1) There are limits on the number of pins for interconnects and transmission capacity between the CPU-mounted package substrate and a motherboard.
2) They require power-consuming loss-compensation circuits and re-timers due to a significant weakening of electrical signals depending on the distance between the CPU and optical transceiver.

To address these issues, an on-package optical interconnect that we are developing has the following characteristics [**Figure 1 (c)**]:

1) A signal is transmitted directly to and from the package substrate via an optical fiber, overcoming the limitation on the number of pins for interconnects.
2) The electrical signal transmission distance between the CPU on the substrate and the optical transceiver (approximately 10–20 mm) is shorter compared to conventional technologies, and it does not require power-consuming loss-compensation circuits or re-timers.

This on-package optical interconnect requires the optical transceiver to be mounted on the package substrate. This in turn means the electrical circuits and other parts in the optical transceiver need to have smaller footprints and lower power consumption, while achieving a packaging structure that realizes high-density integration.

In silicon (Si) photonics, the conventional semiconductor process is applied to optical devices. The technology has the following advantages. First, it integrates extremely small optical devices due to the high refractive index contrast between Si, as the core material of the optical waveguide, and its surrounding materials. Second, it has a very low optical loss, because of the ultrafine processing on a nanoscale. And third, it has a low cost and can be mass produced using the very large Si substrate and existing CMOS facilities.[1), 2)]

In this paper, we describe the ultra-small optical device based on Si photonics technology, and the 28 nm CMOS-based electrical circuit that can operate at high speed with low power consumption. We also report on the results of testing our prototype 25 Gbps optical transceiver with 6 channels (Ch), developed for the on-package optical interconnect, realized through the high-density packaging technology.

## 2. On-package optical interconnect

We will explain the packaging structure of the optical transceiver, designed to realize an on-package optical interconnect. This interconnect contains an optical transceiver mounted on the CPU packaging substrate, as mentioned above. This requires the transceiver to have a smaller footprint, in other words, high-density integration of optical transceivers is needed. To address this challenge, we developed a

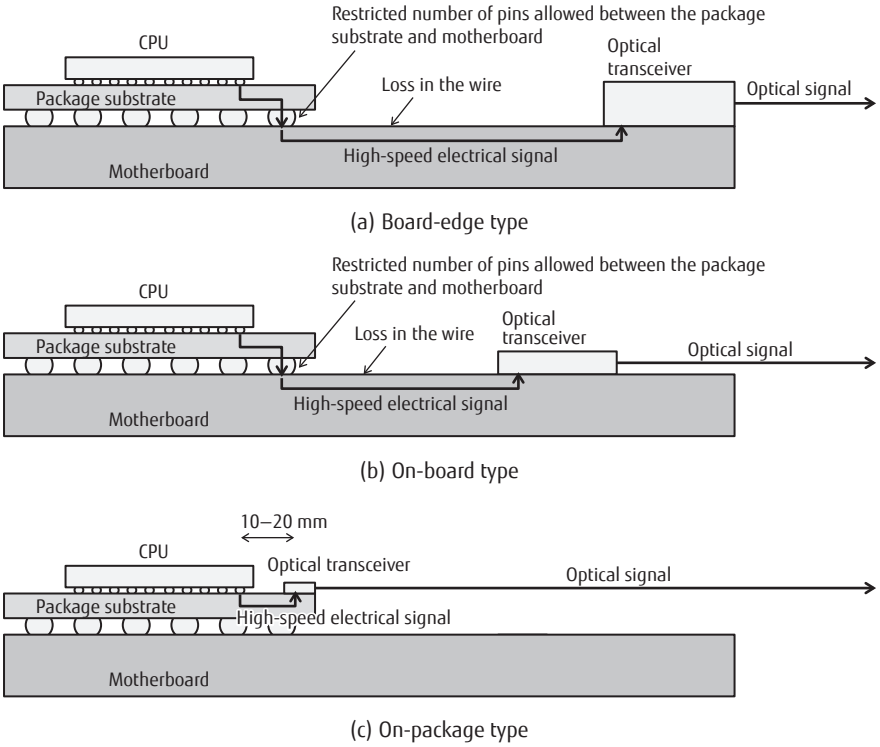
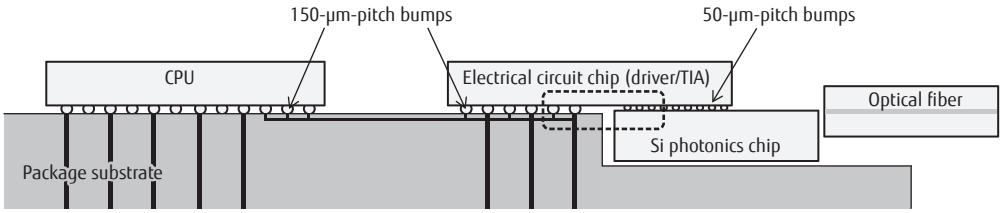



**Figure 1**
**Structure of optical interconnects.**

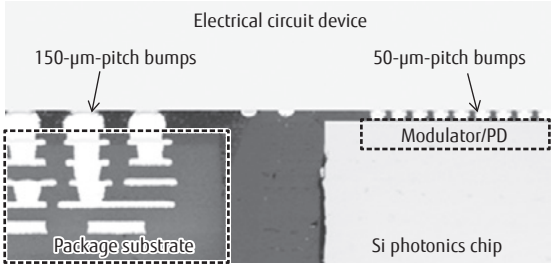
bridge structure as shown in **Figure 2 (a)**.[3] The optical transceiver for the on-package optical interconnect needs a high-density integration of optical transceivers, and easy optical-fiber connection for low cost and high productivity. The bridge structure we proposed comprises the following:

1) A Si photonics chip that integrates an optical modulator to produce an optical intensity-modulated signal, and a photodetector (PD) that outputs the photo current signals corresponding to the input optical modulated signal.
2) A driver for driving the optical modulator and a transimpedance amplifier (TIA) for converting the photo current generated in the PD into a voltage signal.
3) A packaging substrate that supplies high-speed transmission and power.

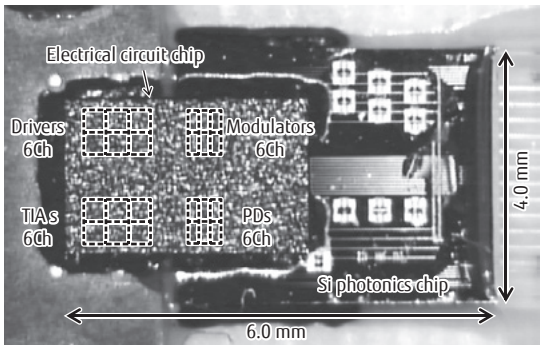
In this structure, the Si photonics and packaging substrate are bridged with the electrical circuit. The interface between the packaging substrate and the electrical circuit chip, and the chips of the electrical circuit and Si photonics, are formed using solder bumps. Conventional wire bonding has a limit in terms of packaging density because the chip pads can only be arranged one-dimensionally between the chips or between the chip and substrate. Also, a higher electrical transmission speed would pose a problem in terms of the signal transfer characteristics and impedance of the wire. The bridge structure we proposed enables two-dimensional connection by solder bumps to connect the electrical circuit chip and packaging substrate, which supply power and high-speed signal as stated above. Also, the bumps realize a connection of only several μm, much shorter than wire bonding, which would be one to several mm, and they make it easier to supply high-quality power and signals. Regarding the optical fiber connectivity, Si photonics chips are embedded in the packaging substrate formed into a groove, and they can be mounted with the optical plane are facing up. This allows an optical fiber to be connected on the edge or surface of the Si photonics chips. **Figure 2 (b)** shows a cross-sectional view of the connection part in the bridge structure, indicated in Figure 2 (a) with a dotted line. The electrical circuit chip and packaging substrate are connected with bumps at a pitch of 150 μm, to ensure a good-quality power supply in particular, as well as to buffer the differences in thermal expansion coefficient between Si and the organic




(a) Schematic diagram of the bridge structure




(b) Cross-sectional view of the bridge structure




Note: Modulators and PDs are formed on the Si photonics chip

(c) Top view of devices mounted using the bridge structure

**Figure 2**
**Bridge packaging.**

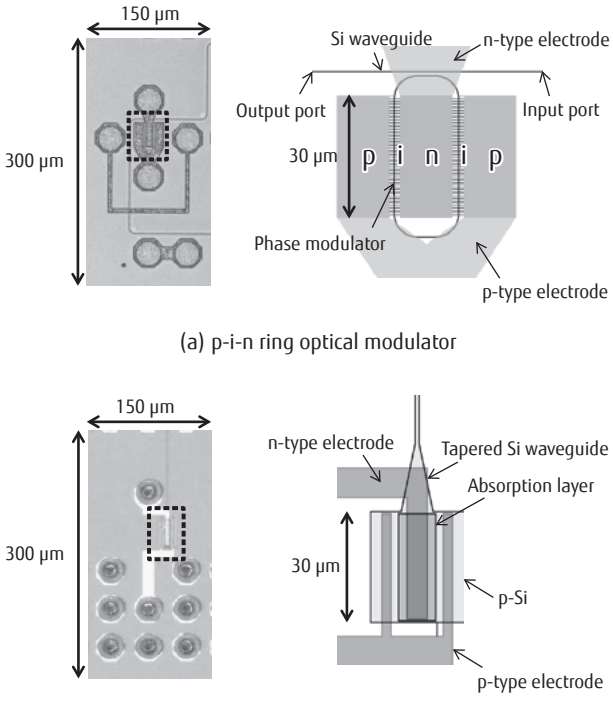
substrate. By contrast, the electrical circuit chips and Si photonics chips are connected with 50-μm-pitch ultra-small bumps, to allow for high-density integration of optical devices, and also because this reduces the parasitic capacitance, which in turn reduces the power loss. These technologies, together with the ultra-small optical device (up to 30 μm), which we will explain in the following section, make the world's highest-level high-density integration possible. The specifications are a footprint of 4.0 by 6.0 mm (24 $mm^2$) with 6 channels of 25 Gbps—6.25 Gbps/$mm^2$, as shown in **Figure 2 (c)**.

## 3. Key technologies

This section describes the key technologies for our prototype optical transceiver. For this prototype, we used a microring optical modulator (to convert the electrical binary signal to an optical intensity-modulated signal), which has a small footprint and a low power consumption, as an optical modulator of the transmitter. In the backbone system, a Mach-Zehnder (MZ) optical modulator is widely used because of its large operating wavelength range and robustness against temperature fluctuations. However, the MZ modulator has a device length of several hundred micrometers to several millimeters, and the modulation efficiency ($V\pi L$)[note 1)] is also insufficient (1 to several V·cm).[4)] By contrast, the ring modulator of Si photonics can be miniaturized significantly thanks to the large refractive index contrasts between Si, as the core material of the optical waveguide, and its surrounding materials. Moreover, due to the optical resonance effect, it is also highly efficient. In particular, the ring modulator used in our prototype has the p-i-n type[note 2)] waveguide structure, and with its modulation efficiency $V\pi L$ at 0.028 V·cm,[5)] it is more efficient than the MZ modulator or p-n type ring optical modulators.[6)] However, the p-i-n type modulators had poor frequency response at high-frequency regions due to their large junction capacitance. To address this problem, we developed emphasized driver circuits. The circuits emphasize a rise-and-fall edge that contains a high-frequency component, which was achieved by dividing the drive signal into two and delaying one before re-synthesizing them. This driver circuit compensates the frequency response of the ring optical modulator, maintaining both the modulation efficiency and high-frequency characteristics. **Figure 3 (a)** shows a photograph and schematic view of the prototype p-i-n type ring optical modulator. The phase modulator region of this p-i-n ring optical modulator is only 30 μm long. This can realize an ultra-small modulator, as the footprint can be miniaturized to dimensions of 50 by 130 μm, even including the electrodes.

We will now describe the optical receiver. We applied a p-i-n Germanium (Ge) PD for the optical receiver.[7)] Ge has a wide range of absorption bands, and Ge can be grown on the Si substrate epitaxially. Therefore, Ge is promising as a material for an absorption layer in a Si photonic receiver.

PD needs to have a small footprint, low-resistance/capacitance (high-frequency response) and a high optical sensitivity in a wide wavelength range. The sensitivity may be improved by upscaling PD




(a) p-i-n ring optical modulator

(b) p-i-n Ge-PD with integrated waveguide

**Figure 3**
**Si photonics devices.**

note 1) One of the properties of an optical modulator. The value is obtained by multiplying the required voltage for π phase-shift by the length of the phase modulator. A smaller figure indicates better conditions.

note 2) Junction structure with p-semiconductor and n-semiconductor bound with an i-semiconductor between them.

devices, but this would be a disadvantage in terms of the footprint and device capacities, and would cancel out the benefit. Similarly, the optical sensitivity and high-frequency response property may be compensated somewhat by adopting a receiver circuit design such as TIA, but this, again, will be a trade-off for power consumption and receiving circuit area in the transceiver's overall system. In this prototype, we adopted a comprehensive design for PDs and TIAs and optimized the design within the limited areas for the PD and circuit. The PD involves a tapered input optical waveguide, which makes it possible to have a uniform and effective coupling with the Ge absorption layer. In this way, we achieved the following: a miniaturizing of down to 30 μm in length, and 10 μm in width, with high optical sensitivity of 0.8 A/W in the wide wavelength range from 1470 to 1570 nm, and a high-speed response at 20 GHz. **Figure 3 (b)** shows a photograph and schematic view of the prototype waveguide-integrated p-i-n Ge-PD. The length of Ge-PD is 30 μm, as stated earlier, while the overall footprint including its electrodes is 50 by 180 μm, just as small as our optical modulator. The noise resistance was improved by introducing pseudo-differential operation and noise-offset cancellation, and also the frequency response was improved by inductor peaking in the receiver circuit. With these improvements, a frequency response of 20 GHz with a transimpedance gain of 65 dB is expected. As a result, a receiver sensitivity of -7.25 dBm under the conditions of 0.8 A/W PD sensitivity and extinction ratio of 3 dB can be anticipated.

## 4. Characteristics of developed optical transceiver

This chapter describes the characteristics of the 25 Gbps optical transceiver adopted for the prototype Si photonics optical transceiver. We evaluated its characteristics by observing the signal waveforms of the transceiver, and measuring the input power dependence of bit error ratio. An overview of the measurement system is shown in **Figure 4 (a)**. We use an external light source with a wavelength of 1.55 μm in this test. A probe is applied, through which the 25 Gbps electrical signal was input/output externally. The relative positioning of the probe and the transceiver represents that of a CPU and an optical transceiver, with the distance between them being 10 mm. There are no loss compensation circuits or re-timers.

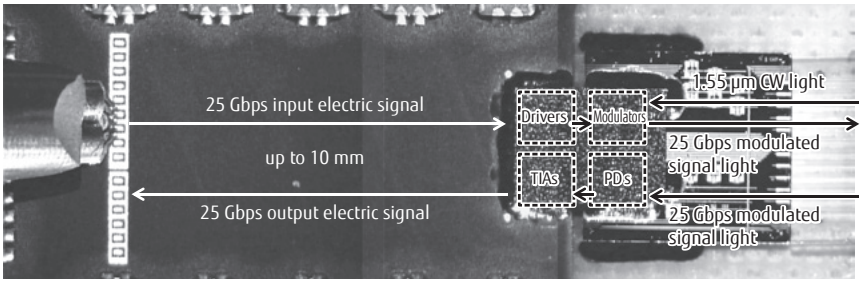
An optical modulator regulates a continuous wave (CW) signal light input from an external light source, and outputs a 25 Gbps modulated optical signal. The optical receiver takes the 25 Gbps modulated signal into the PD, which generates a current signal, and it is in turn converted to a voltage signal by TIA, to output a 25 Gbps electrical signal.

**Figure 4 (b)** shows the waveform (eye pattern)[note 3)] of the optical intensity-modulated signal coming from the Si photonics chip. A high dynamic extinction ratio of 6.5 dB and clear eye opening are observed. The output electrical signal waveform from the electrical circuit chip is shown in **Figure 4 (c)**. Like the optical modulator signal waveform, a clearly opened eye pattern was obtained. The output amplitude was 160 mV, as intended by design.

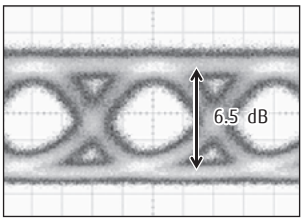
**Figure 4 (d)** shows the power dependence of the bit error ratio of the electrical signal output from optical receiver. As for the bit error ratio, we adopted a ratio of $10^{-12}$, required for conventional transmission systems, to deem the data free from errors. Higher sensitivity is verified if the bit error ratio of $10^{-12}$ is achieved at a lower intensity of the input light. Due to the high sensitivity in PD and high noise resistance in TIA, we achieved error-free operation at an input power of as low as -9.1 dBm, as shown in Figure 4 (c).

The error-free operation was achieved with lower input power than the designed receiver sensitivity. This was achieved possibly because the extinction ratio of the input modulated signal was greater than the design. The power consumption turned out to be 73 mW for the optical transmitter, and 50 mW for the optical receiver, excluding the power consumed by the light source. Their power efficiencies are at 2.9 mW/Gbps and 2.0 mW/Gbps, respectively.[8)] We compared these performances with several reports of other research projects, as shown in **Table 1**[9)–12)] The results show that we have achieved the world's best power efficiency and receiver sensitivity with this prototype Si photonics optical transceiver.

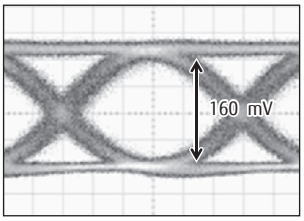
note 3) A diagram in which binary data between 0 and 1 are superposed by cycles over a certain timeframe. It is so called because the pattern looks like a series of eyes between a pair of rails, and these eyes should look as if they are open to prove that the transmitted data have few errors.



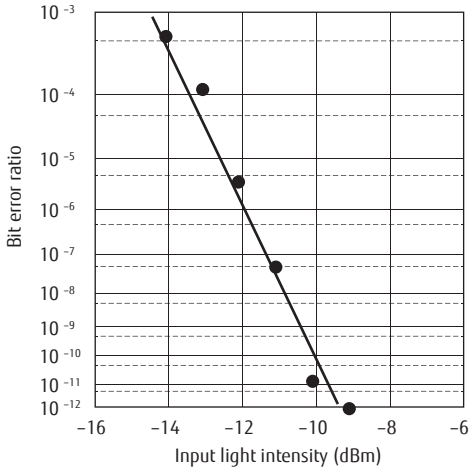

(a) Overview of the measurement system




(b) Optical signal waveform of 25 Gbps (transmitter output)




(c) Electrical signal waveform of 25 Gbps (receiver output)




(d) Bit error ratio dependent on light input intensity

**Figure 4**
**Characteristics of developed transmitter and receiver**

## 5. Conclusion

This paper reported the developed technology of a Si photonics optical transceiver at Fujitsu and Fujitsu Laboratories, in an attempt to realize a small, low-power, on-package optical interconnect. We are expecting to apply this technology to inter-CPU optical interconnects for high-end servers and next-generation supercomputers. Considering factors of power and signal supplies, integration density, and optical fiber assembly, we developed a bridge structure, which required no wiring, and enabled two-dimensional, high-density bonding, in which it is easy to connect the device with optical fibers. This structure made it possible to densely integrate an ultra-small optical transmitter and optical receiver, with the former consisting of a p-i-n microring optical modulator with high modulation efficiency ratio and bandwidth compensation driver circuit, and the latter consisting of p-i-n Ge-PD with high-light-sensitive integrated tapered waveguide and high-speed receiver circuit with high noise resistance. The integrated density was the world's highest at 25 Gbps with 6 channels, which corresponds to 6.25 Gbps/mm$^2$ on a 4.0 by 6.0 mm footprint. The measurement results of the optical signals at 25 Gbps yielded excellent eye opening outcomes for both the transmitter and receiver. Also, error-free operation was verified at an input light power of -9.1 dBm. Moreover, the power efficiency of the transmitter and receiver were 2.9 and 2.0 mW/Gbps, respectively; thus both demonstrate the world's top-class performance. Further challenges include adding functions by integrating the laser light source and control mechanisms, and enhancing the transmission capacity by increasing the number of channels included. After these have been achieved, it will be possible to

**Table 1**
**Comparison of performance characteristics of Si photonics optical transceiver.**

| Item \ Researcher / academic conference | | Buckwalter JSSC 2012[9] | Rosenberg IPC 2013[10] | Takemoto ISSCC 2013[11] | Yashiki OFC 2015[12] | This work |
|---|---|---|---|---|---|---|
| Process technology | | 130 nm SOI | 90 nm SOI | 65 nm CMOS | 28 nm CMOS | 28 nm CMOS |
| Electricity/photonic integration | | Monolithic | Monolithic | Hybrid | Hybrid | Hybrid |
| Data rate (Gbps) | | 25 | 25 | 25 | 25 | 25 |
| Transmitter | Operation voltage (V) | 0.3/-1.2/±1.5 | 1.5/3.0 | – | 3.3/1.0 | 0.9/1.8 |
| | Modulator | p-n ring | p-n ring | – | p-n MZ | p-i-n ring |
| | Dynamic extinction ratio (dB) | 6.9 | 3.5 | – | 4.6 | 6.5 |
| | Power efficiency (mW/Gbps) | 7.2 | 5.5 | – | 3.1 | 2.9 |
| Receiver | Operation voltage (V) | 1.2 | – | 3.3/1.0 | 3.3/1.0 | (0.9) |
| | Sensitivity (dBm) *bit error ratio = $10^{-12}$ | -6.0 | – | -9.7 | -4.9 | -9.1 |
| | Power efficiency (mW/Gbps) | 1.92 | – | 4.9 | 1.8 | 2.0 |

commercialize the device.

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