Impact of Nitrogen Profile in Gate Nitrided-Oxide on Deep-Submicron CMOS Performance and Reliability

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Silicon dioxide has been used for the gate insulator in CMOS with gate lengths down to 0.25 µm. However, when we enter the sub-0.18 µm era, nitrogen atoms must be incorporated into the silicon dioxide to prevent an undesirable penetration of boron atoms from the gate electrode to the Si substrate. In this paper, we describe the effects of the nitrogen atom profile on CMOS performance and reliability and clarify the mechanisms underlying these effects. We show that high-performance, high-reliability CMOSFETs can be achieved by using a newly developed nitrided-oxide process that features a 900°C gate nitrided-oxide and establishes different nitrogen concentrations between the gate and extension area. When we enter the sub-100 nm-gate-length era of CMOS, we will need to replace thermal nitridation for the gate oxide with an alternative nitridation process, for example, plasma nitridation.

1. Introduction

Without an exquisite combination of silicon-dioxide (SiO_2) and Si, we could not have enjoyed the benefits of IT (Information Technology) technologies based on state-of-the-art CMOS (Complementary Metal-Oxide-Semiconductor) technology.

As long as CMOS gate lengths stay around 0.25 µm, we do not need to worry about using silicon dioxide as a gate-insulator. However, when we enter the sub-0.18 µm-gate-length era of CMOS, for the first time we face the need to replace SiO_2 with another gate insulator. To achieve a high-performance, 0.18 µm-gate-length surface-channel p-MOSFET, we need to use p^+-poly-crystalline-silicon for the gate material.[1] However, boron penetration from the p^+-poly-crystalline-silicon gate into the underlying silicon substrate degrades device operation. This degradation includes instability in the threshold voltage (V_{th}), an increase in the charge-trapping rate, a decrease in low-field mobility,[2)-4)] and a reduced current drivability due to depletion of the poly-crystalline-silicon electrode.[5]

Fujitsu has a long history of comprehensively studying nitrided-oxide gate dielectrics,[6),7)] and to address these issues caused by boron diffusion, we have tried to replace gate SiO_2 with nitrided-oxide. Nitrided-oxide gate dielectrics (Gate-NO) have been used for dual-gate CMOSFETs with deep submicron channel lengths because of their high boron blocking ability[8),9)] (**Figure 1**) and hot carrier immunity.[10),11)] However, the most serious problem with Gate-NO is that it deteriorates p-MOSFET drivability.[12] Preventing extension dopants, especially boron, from diffusing outward into the sidewall and increasing the parasitic series resistance (Rext) is expected to be another important issue. To address these issues, we inserted a nitrided-oxide (Ex-NO) between the extension area and sidewall as a blocking layer (**Figure 2**). We devised a novel way to independently optimize the nitrogen profile and content for the Gate-NO and Ex-NO to suppress the deg-

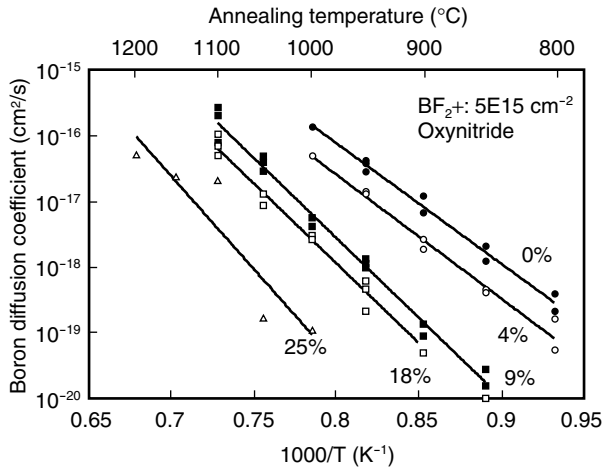


Figure 1
Boron diffusion coefficient in oxynitride.

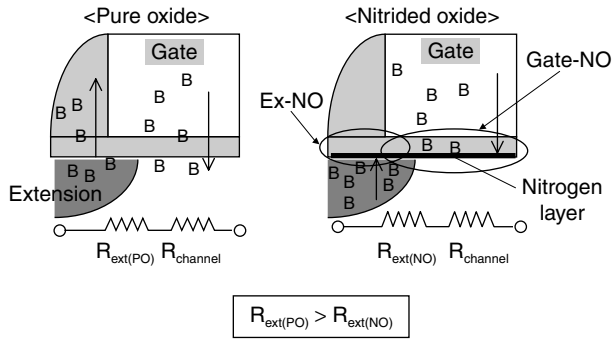


Figure 2
Schematic cross section of p-MOSFET described in this paper.

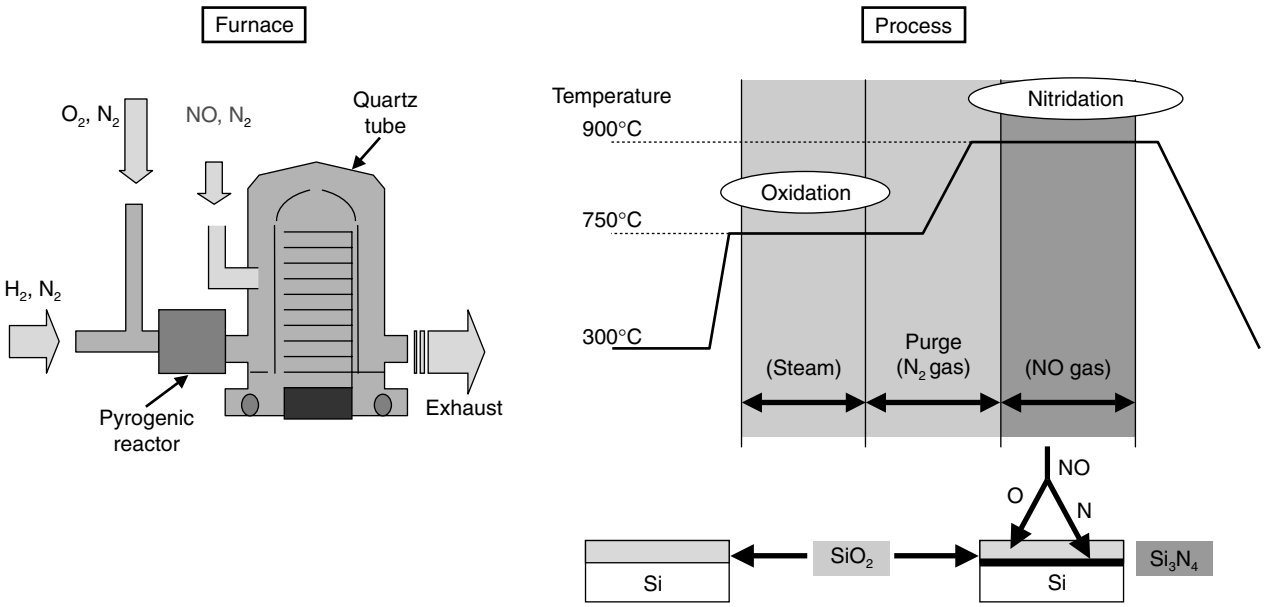


Figure 3
Gate nitrided-oxide process.

radation of p-MOSFET drivability and the outward diffusion of extension dopant.

2. Experiments

The gate insulator formation furnace and process are shown in **Figure 3**. As a control, gate oxide was thermally grown in the furnace at 750 to 800°C. Gate-NO was grown by annealing thermal oxide in NO or N_2O gas ambient at 800°C or 900°C. Ex-NO was also formed with NO in the same furnace after gate electrode formation and residual gate oxide removal. The process flow of the MOSFET is shown in **Figure 4**. After isolation, a thin (3.5 to 5.5 nm) gate dielectric was grown. The gate dielectric thickness was determined by C-V measurement. Dual gate doping was carried out by B + and P + implantation after poly-Si deposition (180 nm). Shallow extension was performed by low-energy implantation after Ex-NO formation. Sidewall formation (CVD-SiO_2)

was followed by deep S/D implantation and RTA (Rapid Thermal Annealing) at 1000°C.

We examined the nitrogen depth profile using SIMS (Secondary Ion Mass Spectroscopy), the nitrogen chemical bonding state using XPS (X-ray Photo-emission Spectroscopy), and the interface property using charge pumping current measurement. We evaluated the characteristics of 0.2 µm CMOSFETs and extracted the mobility and series resistance using the shift and ratio method.[13] We also evaluated the hot carrier immunity for n-MOSFETs.

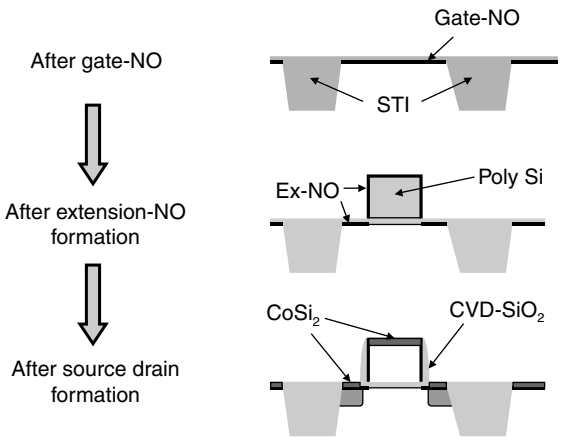


Figure 4
Process flow of MOSFET.

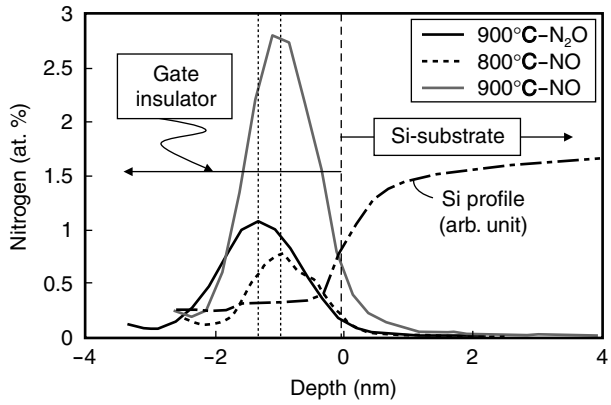


Figure 5
Nitrogen depth profile for 900°C-NO, 800°C-NO, and 900°C-N_2O measured by secondary ion mass spectroscopy.

3. Results

3.1 Nitrided-oxide film properties

We examined the nitrogen depth profile by SIMS for three kinds of nitrided-oxide: 900°C-NO, 800°C-NO, and 900°C-N_2O (**Figure 5**). We also studied the nitrogen chemical bonding state using XPS. **Figure 6** shows N_{1s} spectra at various take-off angles for the 900°C-NO and 800°C-NO. The 900°C-NO has a sharp peak at about 398 eV, which corresponds to the $Si_3 \equiv N$ bond in CVD-Si_3N_4.[14] On the other hand, the 800°C-NO has two peaks: one at about 398 eV and another at about 399 eV.

The intensity of the 398 eV peaks increases with the take-off angle, and the intensity of the 399 eV peak decreases with the take-off angle. This indicates that the 398 and 399 eV peaks correspond, respectively, to a nitrogen-related bond near the interface and a nitrogen-related bond in the bulk nitrided-oxide.[15] As the thickness of the 800°C-NO is increased, the binding energy (BE) around 399 eV increases, but the BE around 398 eV remains almost constant (**Figure 7**). This energy shift might be caused by the X-ray induced charge-up effect,[16] implying that the 399 eV peak also corresponds to $Si_3 \equiv N$ bonds and some nitrogen atoms exist away from the interface. These results suggest that nitrogen atoms exist both at the interface and in the bulk in the 800°C-NO

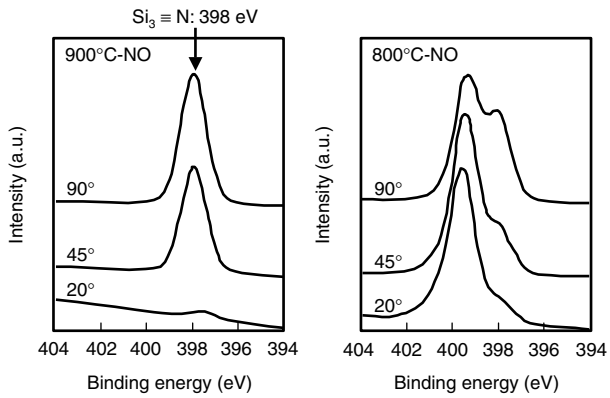


Figure 6
N_{1s} photoelectron spectra for various take-off angles of 900°C-NO and 800°C-NO by XPS.

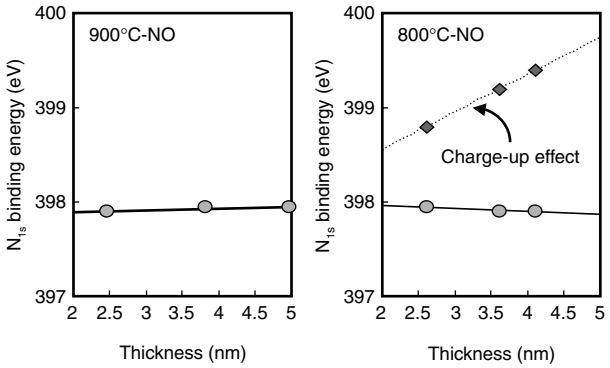


Figure 7
Dependence of N_{1s} binding energy on oxynitride thickness for 900°C-NO and 800°C-NO by XPS.

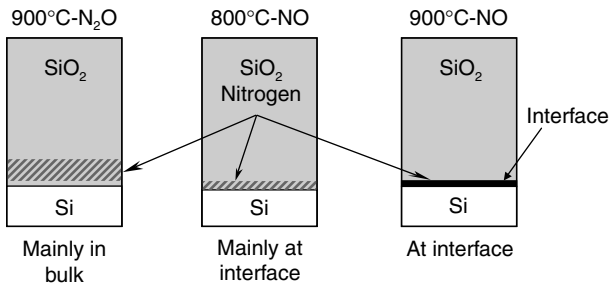
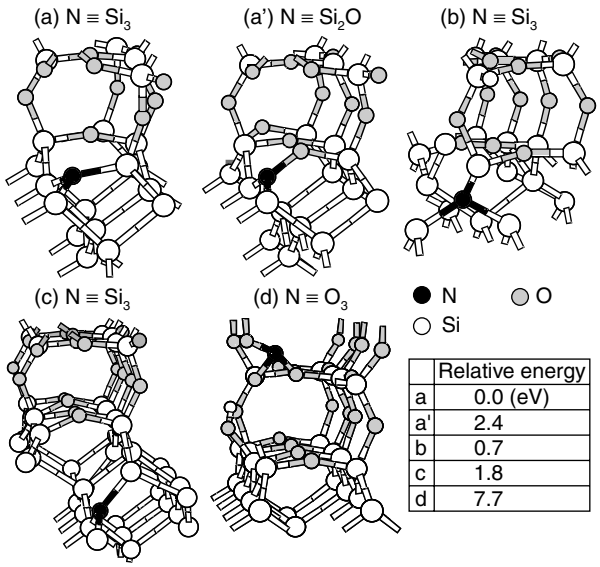


Figure 8
Schematic cross section of nitrided oxide showing the location of nitrogen.



	Relative energy
a	0.0 (eV)
a'	2.4
b	0.7
c	1.8
d	7.7

Figure 9
Three-coordinated-N-configurations. (a) $Si_3 \equiv N$ at the interface, (a') $Si_2O \equiv N$ at the interface, (b) $Si_3 \equiv N$ at the second layer in the substrate, (c) $Si_3 \equiv N$ at the third layer in the substrate, and (d) $O_3 \equiv N$ in the SiO_2 region.

samples, but only at the interface in the 900°C-NO) samples.[17] The XPS spectra for the 900°C-N_2O mainly consisted of a 399 eV peak, showing that nitrogen atoms are located in the bulk (**Figure 8**).[18]

A theoretical analysis based on first-principle calculation also confirms that the $Si_3 \equiv N$ bonds at the interface are the most stable and higher temperature thermal treatments induce nitrogen atoms to pile up at the SiO_2/Si interface (**Figure 9**).[19]

3.2 Nitrided-oxide interface properties

Figure 10 shows the charge pumping current[20] of n-MOSFETs and p-MOSFETs with various gate insulators. The peak nitrogen concentration of nitride-oxide was confirmed to be 0.8 atomic %. The charge pumping currents of the 900°C-NO n- and p-MOSFETs are less than those for the other samples. This implies that the N_{it} for 900°C-NO is the smallest. Furthermore, compared with the n-MOSFETs, there is a remarkable V_{th} shift in the p-MOSFETs. This V_{th} shift was not caused by a fixed charge in the gate dielectric, because the same shift was not observed in the n-MOSFETs. Moreover, the V_{th} of the gate oxide is shifted positively from the V_{th} of the gate nitrided-oxide. Therefore, we consider that the V_{th} shift was caused by boron penetration. Thus, the gate nitrided-oxide suppressed the V_{th} shift caused by boron penetration. **Figure 11** shows the dependence of N_{it} on N_{peak} in the n- and p-MOSFETs. Among the n-MOSFETs, in this range of N_{peak} the N_{it} of the 900°C-NO sample was lower than that of the other samples, even the pure oxide sample. Also, the N_{it} of all three nitrided-oxide samples increased as N_{peak} increased. Among the p-MOSFETs, the 900°C-NO sample with a 0.8 atomic % N_{peak} had the smallest N_{it}, indicating that it had better interface characteristics than the other samples.

According to the theoretical analysis mentioned above,[19] the interface $Si_3 \equiv N$ configuration

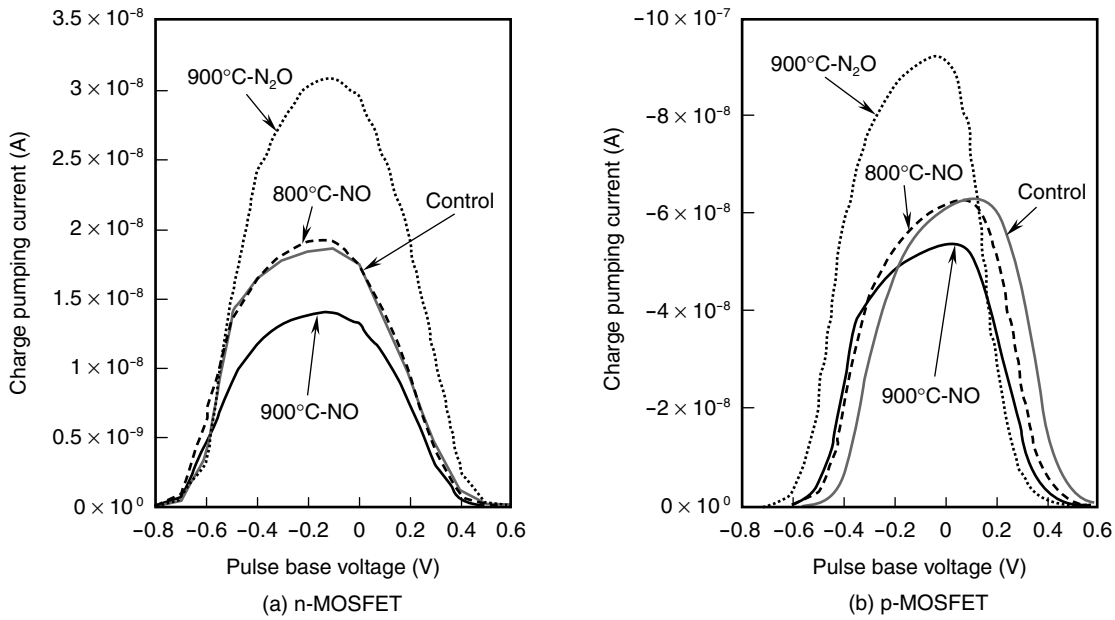


Figure 10
Charge pumping current of n-MOSFETs and p-MOSFETs with various gate insulators.

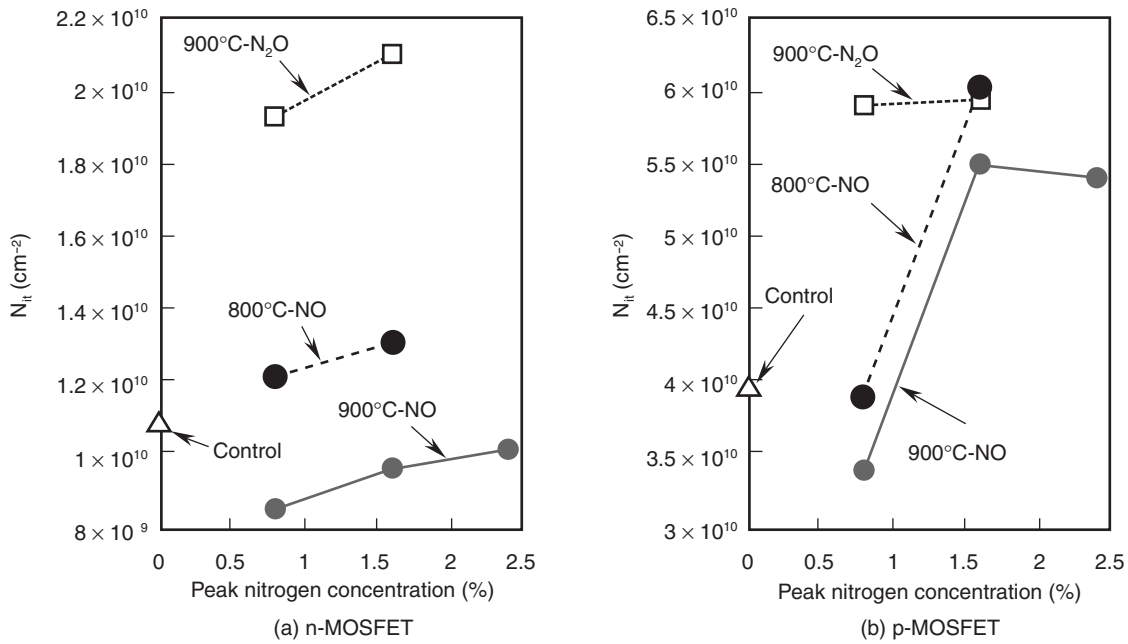


Figure 11
Dependence of interface state density obtained by charge pumping measurement on peak nitrogen concentration in n- and p-MOSFETs.

of (a) has no gap states. Substituted N atoms in configurations (b) and (c) generate dangling bonds at the Si atoms near the N atoms, and the dangling bonds create gap states and work as hole trapping sites. When we increase the nitrogen atom content above 0.8%, nitrogen atoms can no longer be accommodated at the SiO_2/Si interface, which might create gap states, especially in p-MOSFETs.

3.3 Characteristics of CMOSFETs with the same NO concentrations in the gate and extension

Figure 12 shows the Ion vs. Ioff characteristics for a 0.2 µm p-MOSFET. A significant 50% reduction in Ioff has been achieved using 1.5% NO compared with pure oxide. This remarkable reduction in Ioff might be due to the suppression of dopant (boron) diffusion in the lateral direction, owing to the Ex-NO. **Figure 13** shows the mobilities of this p-MOSFET with various gate dielectrics. Surprisingly enough, the nitrogen content can be increased to 1.5% without degrading the mobility characteristics. However, 5.3% NO deteriorates the mobility. The parasitic resistances (Rext) of this p-MOSFET with various dielectrics are shown in **Figure 14**. The decrease of Rext for 1.5% NO compared with pure oxide implies that Ex-NO can effectively suppress the outward diffusion of dopant. This effect is more prominent when the nitrogen concentration is increased to 5.3%.

Figure 15 shows the dependence of device lifetime on the substrate current for n-MOSFETs

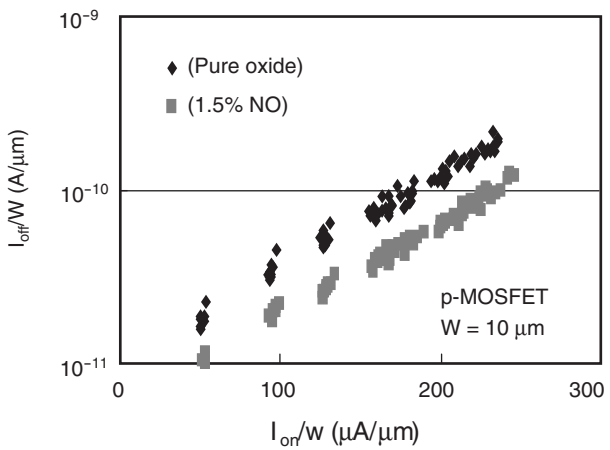


Figure 12
Ion vs Ioff characteristics of p-MOSFET (W = 10 µm).

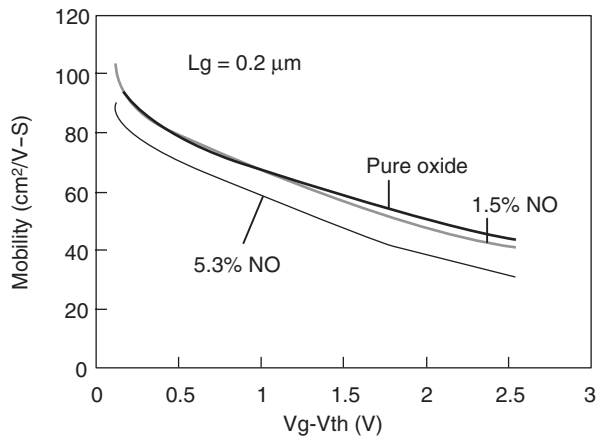


Figure 13
Mobilities of 0.2 µm p-MOSFET with various gate dielectrics obtained by shift and ratio method.

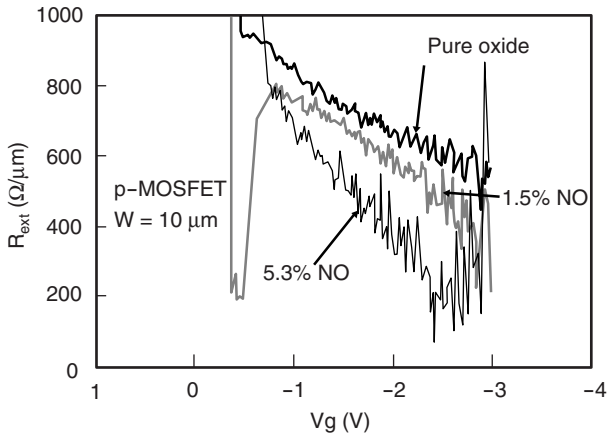


Figure 14
Rext of 0.2 µm p-MOSFET with various gate dielectrics obtained by shift and ratio method. Dopant concentration near the surface of extension area is about 10^{19} atoms/cm^3.

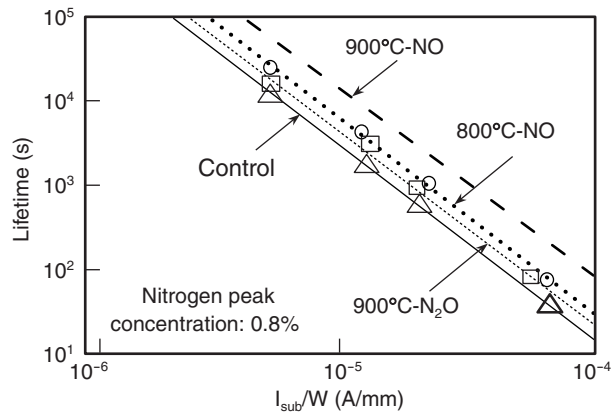


Figure 15
Dependence of device lifetime of n-MOSFET on substrate current under drain avalanche hot carrier stress. Lifetime is defined as the time to reach a 10% degradation in saturation current.

with gate oxide and gate nitrided-oxide under DAHC (Drain Avalanche Hot Carrier) stress. The N_{peak} of the nitrided-oxide is 0.8 atomic %. The lifetime is defined as the time to reach a 10% degradation in the saturation current measured at $V_d = V_g = 2.5$ V, where V_d and V_g are the drain and gate voltages, respectively. The nitrided-oxide, especially 900°C-NO, yielded better hot carrier immunity than the pure oxide. **Figure 16** shows the dependence of N_{it} on N_{peak} for n-MOSFETs after application of hot carrier stress for 10^4 s. N_{it} of the nitrided-oxide is less than that of pure oxide and decreases as N_{peak} increases. This implies that the use of nitrided-oxide suppressed the generation of N_{it} during DAHC stress. Moreover, a superior suppression of hot carrier degradation with 900°C-NO was observed, even when N_{peak} was the same.[21)]

3.4 Characteristics of CMOSFETs with different NO concentrations in the gate and extension

The trade-off problem between mobility and Rext inevitably arises for the same Gate-NO and Ex-NO concentration. The combination of 1.5% Gate-NO and 5.3% Ex-NO successfully increases Ids by 12% in a 0.2 µm p-MOSFET compared to the combination of gate and extension pure oxide (**Table 1**).[22)] As the channel length is reduced, the contribution of Rext becomes larger. For p-MOSFETs with gate lengths below 0.1 µm, a further increase in Ids could be expected by suppressing unfavorable boron diffusion from the extension area. Enveloping the boron extension area with implanted nitrogen (N-tub) (**Figure 17**) is also effective for suppressing the unfavorable boron diffusion and clearly verifies the validity of this idea[23)] (**Figure 18**).

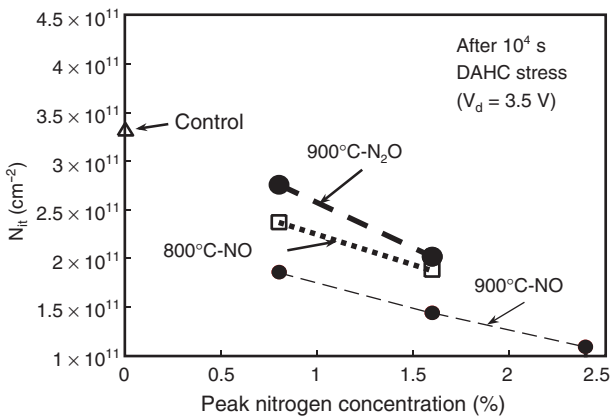


Figure 16
Dependence of interface state density of n-MOSFET obtained by charge pumping measurement on peak nitrogen concentration after application of drain avalanche hot carrier stress for 10^4 s.

4. Gate insulator in sub-100 nm node

When we fabricate devices with gate lengths of less than 100 nm, we have to reduce the gate oxide thickness to less than 1.2 nm,[24)-26)] which results in a serious increase in gate leakage current. Increasing the dielectric constant of the gate

Table 1
I_{on} and Ioff of p-MOSFET with various Gate-NO and Extension-NO.

N_{peak} concentration (%)		Relative ratio (pure oxide = 1)	
Gate-NO	Ex-NO	I_{on}	I_{off}
0	0	1	1
1.5	1.5	1.07	0.52
1.5	5.3	1.12	0.50

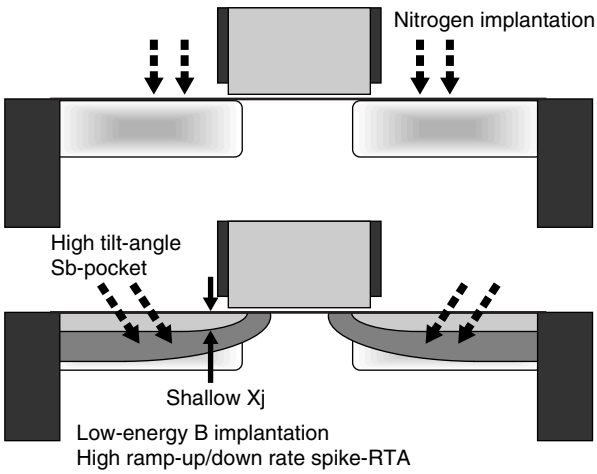


Figure 17
Schematic of N-tub design concept.

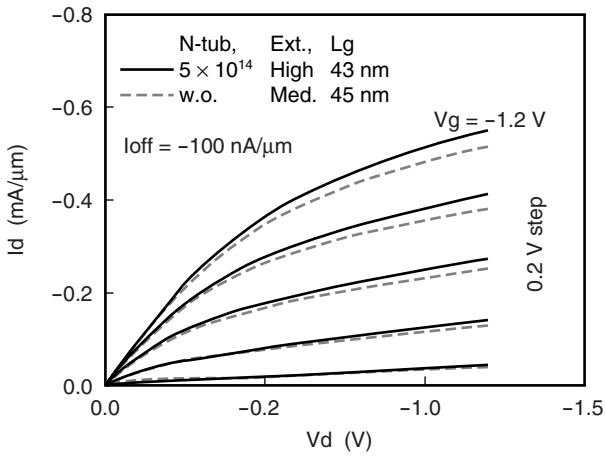


Figure 18
Id-Vd characteristics of N-tub MOSFET.

Table 2
Change of gate oxide process.

Device generation	Lg>250 nm	180 nm>Lg>130 nm	Lg<100 nm
Gate oxide thickness	Tox>5.5 nm	4.0 nm>Tox>1.8 nm	Tox<1.2 nm
Structure	O_2 Si substrate	O_2, NO Si substrate	O_2, NO plasma N_2 Si substrate
N distribution	None	Near Si substrate	Near Si substrate +SiO_2 surface
Process	Oxidation	Oxidation +NO nitridation	Oxidation +NO nitridation +Plasma nitridation

insulator is an effective way to avoid the leakage current increase.[27] Reducing the gate oxide thickness requires a further ability of gate nitrided-oxide to suppress boron penetration. In general, this further ability might be achieved by increasing the nitrogen content of the nitrided-oxide. However, further increases of the nitrogen content around the gate-oxide/Si-substrate interface enhances Negative Bias Temperature Instability (NBTI).[28)-30)]

Plasma nitridation of the nitrided-oxide has been developed as a promising solution to reduce the gate leakage current and gate-to-substrate boron penetration without enhancing the NBTI, because this process can confine the nitrogen atoms around the top of the gate nitrided-oxide[31] (**Table 2**).

In addition to an aggressive development of new technologies that enable us to fabricate thinner gate nitrided-oxides, a comprehensive understanding of the NBTI mechanism as well as the development of a highly nitrogen-doped gate oxide that is free of fixed charges are strongly anticipated. A theoretical analysis that is tightly linked with precise material research, of course guided by device performance evaluation, might be a solid solution to this keen need to further reduce gate oxide thickness.

5. Conclusions

We showed that a nitrided-oxide gate dielectric grown at 900°C in NO has a nitrogen peak at the SiO_2/Si interface, which has the effect of decreasing the interface state density and suppressing the outward diffusion of extension dopant. We have fabricated a high-performance, high-reliability CMOSFET using a newly developed nitrided-oxide process. The process features 900°C Gate-NO and establishes different nitrogen concentrations between the gate and extension area. In p-MOSFETs, the new process can increase Ids by 12% and decrease Ioff by 50% compared with the case when pure oxide is used. In n-MOSFETs, the new process can significantly improve hot carrier reliability.

When we enter the sub-100 nm-gate-length era of CMOS, we will need to replace thermal nitridation for the gate oxide with an alternative nitridation process, for example, plasma nitridation.

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