Post-K Supercomputer Overview
Post-K supercomputer overview

- Developing “Post-K” as the successor to the K computer with RIKEN
- Developing HPC-optimized high performance CPU and system software
- Selected ARMv8 with SVE ISA for the CPU

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**PRIMEHPC FX10**
- 236.5GF, 16-core/CPU
- 4SIMD, 1TF~, 32+2-core/CPU
- Tofu2 integrated, HMC

**PRIMEHPC FX100**
- Handles millions of parallel jobs
- FEFS: super scalable file system
- MPI: Ultra scalable collective communication libraries
- OS: Lower OS jitter w/ assistant core

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Japan's National Projects

- Operation of K computer
- Post-K
- HPCI strategic apps program
- App. review
- FS projects
- Post-K computer development

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Post-K goals and approaches

Goals
- High application performance
- Good power efficiency
- Application portability
- Advance from K computer and PRIMEHPC FX series
- Good usability for users

Approaches
- Develops a custom high performance & scalable CPU
  - Post-K CPU core design
  - SMaC based Post-K CPU design
- Advances system software for Post-K
- Optimizes for higher application performance and scalability
- Complies with standard specifications for usability and application portability
**Post-K CPU core design**

- Developing high performance CPU adopting ARMv8 with SVE ISA
- Contributing to development of SVE (Scalable Vector Extension) with ARM
- Inheriting and enhancing the preceding CPUs’ functions

### HPC apps acceleration

<table>
<thead>
<tr>
<th></th>
<th>Post-K</th>
<th>FX100</th>
<th>FX10</th>
<th>K computer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Base ISA + SIMD Extensions</strong></td>
<td>ARMv8+SVE</td>
<td>SPARCv9+HPC-ACE2</td>
<td>SPARCv9+HPC-ACE</td>
<td>SPARCv9+HPC-ACE</td>
</tr>
<tr>
<td><strong>SIMD width [bit]</strong></td>
<td>512</td>
<td>256</td>
<td>128</td>
<td>128</td>
</tr>
<tr>
<td><strong>Gather Load and Scatter Store</strong></td>
<td>✔ Enhanced</td>
<td>✔</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>FMA: Floating-point multiply and add</strong></td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td><strong>Packed Single Precision SIMD</strong></td>
<td>✔ Enhanced</td>
<td>✔</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>Math. acceleration primitives</strong></td>
<td>✔ Enhanced</td>
<td>✔ Enhanced</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td><strong>Inter-core barrier</strong></td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td><strong>Sector cache</strong></td>
<td>✔ Enhanced</td>
<td>✔ Enhanced</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td><strong>Hardware “prefetch” assist</strong></td>
<td>✔ Enhanced</td>
<td>✔ Enhanced</td>
<td>✔</td>
<td>✔</td>
</tr>
</tbody>
</table>

*Mathematical acceleration primitives include trigonometric functions, exponential functions, etc.*
SMaC based Post-K CPU design

- Improves Fujitsu’s proven μ-architecture, SMaC (Scalable Many Core) optimized for HPC applications

SMaC example for FX100

**Middle-sized, general purpose, out-of-order, superscalar processor core**
- Good performance for variety of apps
- Low power with power management functions

**Assistant core**
- OS jitter reduction and assistance for IO, async MPI
- Scalable for massively parallel system

**Core Memory Group (CMG), many core building block, ccNUMA thin connection**
- Hierarchical structure for hybrid parallel model
- Optimized area and performance

**Implementation of FX100**
- Core Memory Group
  - Compute Engine (CE)
  - Hardware barrier
  - Shared L2 $\$
  - Dedicated memory controller
- Core Memory Group (CMG)
- Memory

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## Advanced system software for Post-K

- Developing based on co-design scheme with application developers
- Keeping application portability by providing programming environment

### Post-K applications

<table>
<thead>
<tr>
<th>FUJITSU Technical Computing Suite / RIKEN Advanced system software</th>
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<tbody>
<tr>
<td><strong>Management software</strong></td>
</tr>
<tr>
<td>System management for highly available &amp; power saving system operation</td>
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<tr>
<td>Job management for higher system utilization &amp; power efficiency</td>
</tr>
<tr>
<td><strong>Hierarchical file I/O software</strong></td>
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<tr>
<td>Application-oriented File I/O middleware</td>
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<tr>
<td>Lustre-based cluster file system FEFS</td>
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<tr>
<td><strong>Programming environment</strong></td>
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<tr>
<td>XcalableMP</td>
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<tr>
<td>MPI(Open MPI, MPICH)</td>
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<tr>
<td>OpenMP, COARRAY, Math Libs.</td>
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<tr>
<td>Compilers(C,C++,Fortran)</td>
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<tr>
<td>Debugging and tuning tools</td>
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</tbody>
</table>

### Linux OS / McKernel(Lightweight Kernel)

### Post-K system hardware

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Optimizes for higher application performance and scalability

- Develops HPC-optimized technologies
- Enhances the features of K computer, PRIMEHPC FX10/FX100 systems

**Hardware:**
- Fujitsu-designed CPU with SVE
- Tofu 6D mesh/torus interconnect

**System software:**
- McKernel with Zero OS jitter
- Distributed file system FEFS
- Parallelizing compilers
- Tuned MPI libs
- Management software
Complies standard specifications for usability and application portability

- Compliance with ARM standard platform specifications
  - To co-operate ARM/Linux community and utilize system software and OSSs
  - To ensure binary level application portability

- ISA: ARMv8-A with SVE
- System architecture: SBSA level3, SBBR
- Firmware interface: UEFI, PSCI
- API, library: Linux APIs, Standard MPIs, Standard math. libs
- Languages
  - Fully supported: Fortran 2008, C11, C++14, OpenMP 4.5
  - Partially supported: Fortran 2015, C++1z, OpenMP 5.0
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