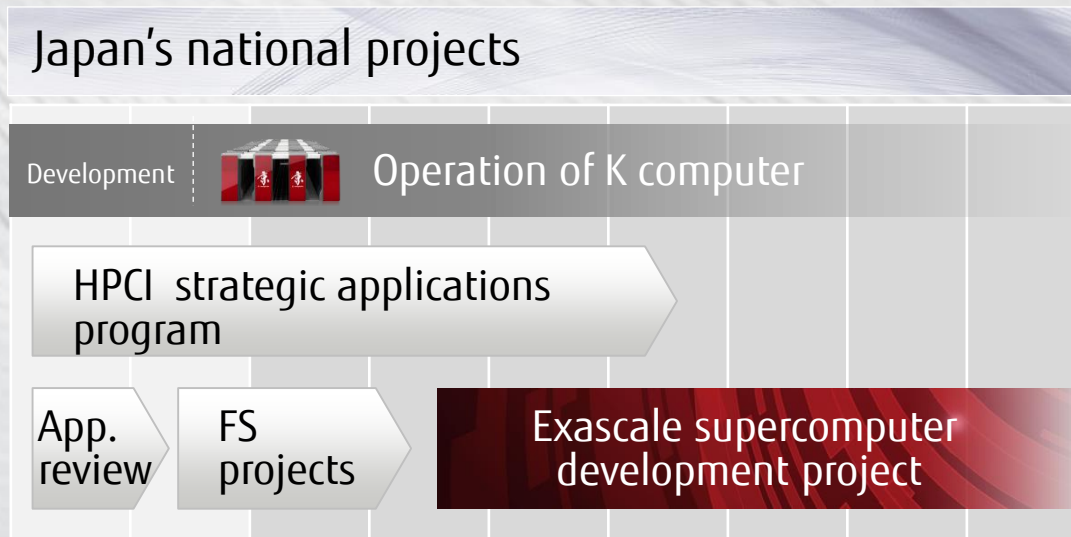
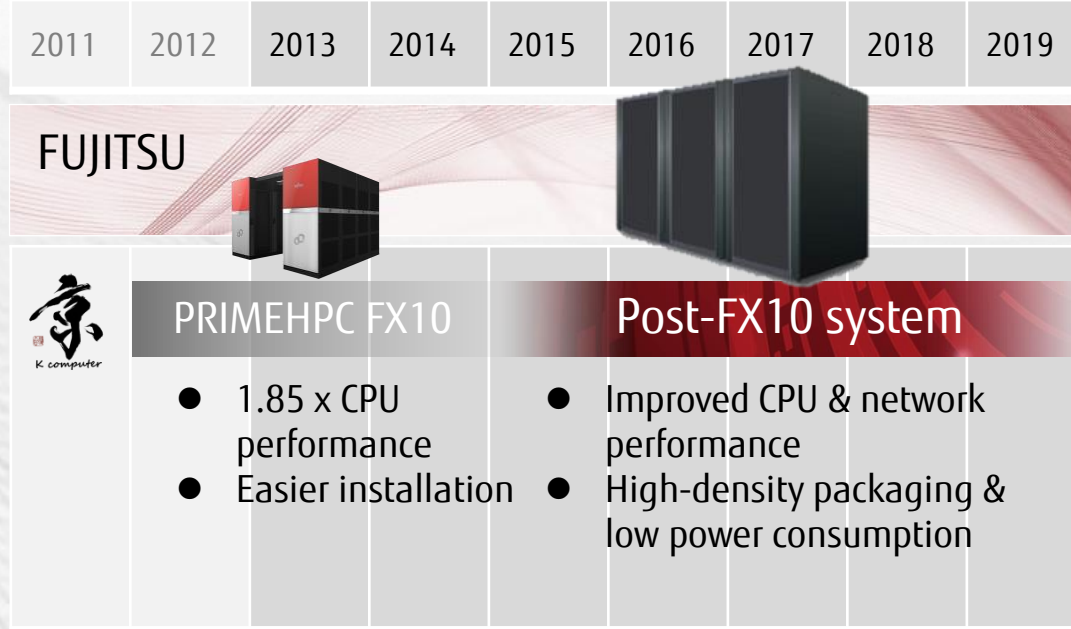


Fujitsu's Approach for Exascale

Toshiyuki Shimizu

June 23rd, 2014

Roadmap and Research for Exascale



■ K computer and PRIMEHPC FX10 in operation

- Many applications running and being developed for science and industries

■ Post-FX10 is coming soon

- CPU and interconnect will inherit K computer architectural concept

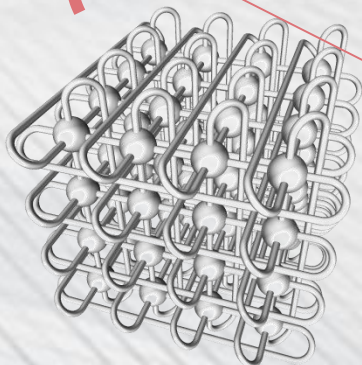
■ R&D for Exascale

- Higher performance and lower power consumption technologies for hardware and software
- Participated in national projects, App. Review and FS, proactively
- Riken is reviewing the plan to drive the Exascale supercomputer development project, referring to the results of FS

Feature and Configuration of Post-FX10

Fujitsu designed SPARC64™ XI fx

- ◆ 1TF~(DP)/2TF~(SP)
- ◆ 32 + 2 core CPU
- ◆ HPC-ACE2 support
- ◆ Tofu2 integrated

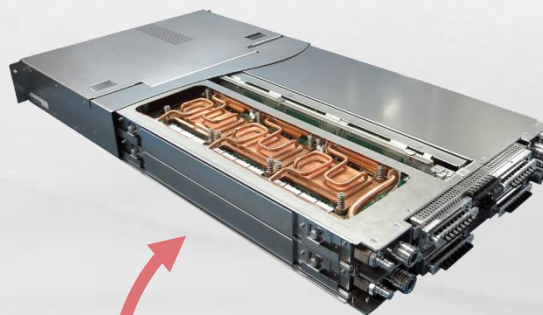


Tofu Interconnect 2

- ◆ 12.5 GB/s×2(in/out)/link
- ◆ 10 links/node
- ◆ Optical technology

Chassis

- ◆ 1 CPU/1 node
- ◆ 12 nodes/2U Chassis
- ◆ Water cooled



CPU Memory Board

- ◆ Three CPUs
- ◆ 3 x 8 Micron's HMCs
- ◆ 8 Finisar's opt modules, BOA, for inter-chassis connections



Cabinet

- ◆ 200~ nodes/cabinet
- ◆ High-density
- ◆ 100% water cooled with EXCU (option)

Feature and Configuration of Post-FX10

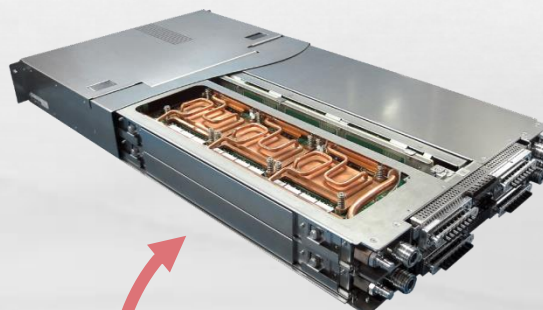
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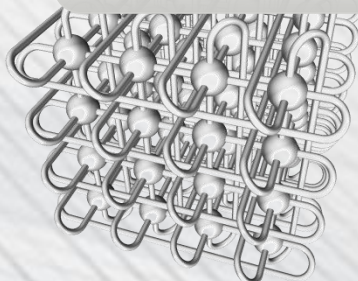


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Same application view as FX10 & K computer



Tofu Interconnect 2

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K computer and Fujitsu PRIMEHPC series

- Single CPU/node architecture for multicore
 - Good Bytes/flop and scalability
- Key technologies for massively parallel supercomputers
 - Original CPU and interconnect
 - Support for tens of millions of cores (VISIMPACT*, Collective comm. HW)

PRIMEHPC Series

FX1

VISIMPACT
Collective comm. HW



CY2008~
40GF, 4-core/CPU

K computer

SIMD extension HPC-ACE
Direct network Tofu



CY2010~
128GF, 8-core/CPU

FX10

HPC-ACE
Direct network Tofu



CY2012~
236.5GF, 16-core/CPU

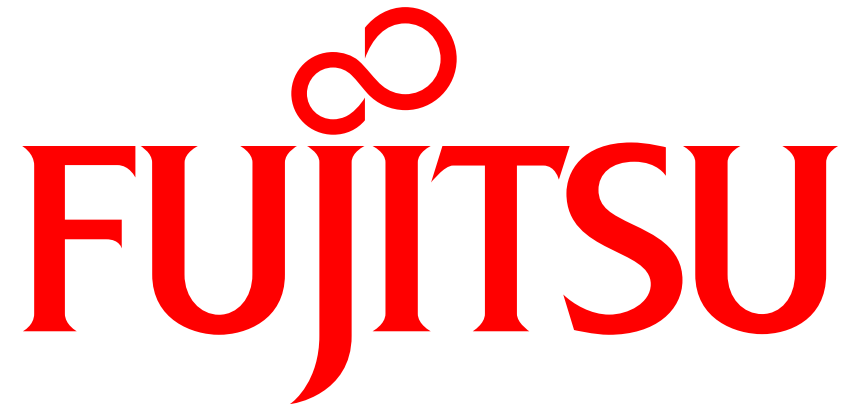
Post-FX10

HPC-ACE2
Tofu interconnect 2
HMC & Optical connections



Coming soon
1TF~, 32-core/CPU

* VISIMPACT: Virtual Single Processor by Integrated Multi-core Parallel Architecture



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