A New Generation 16-core Processor for Supercomputing

SPARC64™ IXfx
Fujitsu Processor Development

SPARC64™
Processor

- L2$ on die
- Non blocking cache
- OOOE
- Superscalar
- Single-chip CPU
- Store ahead
- Branch prediction
- Prefetch
- Cache ECC
- Register/ALU parity
- Instruction retry
- Cache dynamic degradation
- RC/RT/history

Mainframe Processor

Technology generation

SPARC64 IXfx

SPARC64 VIIIfx

SPARC64 VIIIx

GS21 1600

GS8800

GS8800B

GS8800

GS8900

SPARC64 GP

SPARC64 V +

GS21 900

Tr=30M CMOS Cu 130nm

Tr=46M CMOS Cu 180nm

Tr=500M CMOS Cu 90nm

Tr=540M CMOS Cu 90nm

Tr=600M CMOS Cu 65nm

Tr=800M CMOS Cu 65nm

Tr=10M CMOS Al 350nm

Tr=190M CMOS Cu 130nm

Tr=190M CMOS Al 250nm / 220nm

Tr=30M CMOS Cu 180nm / 150nm

Tr=400M CMOS Cu 90nm

Tr=500M CMOS Cu 90nm

Tr=600M CMOS Cu 65nm

GS9600

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**SPARC64™ IXfx**

- Inherited features from SPARC64™ VIIIfx
  - High performance
    - HPC-ACE
    - Embedded memory controller
    - Hardware barrier mechanism
  - Low power
    - Moderate frequency
    - Dynamic/Leakage power reduction
  - High reliability
    - RAS features

- New features
  - Doubled number of cores
  - Doubled size of L2$
SPARC64™ IXfx Core Overview

- **Instruction control Unit**
  - Controls the fetch, issue, and completion of instruction

- **Execution unit**
  - Performs integer and floating-point operations
  - Occupy the large part of a core
  - Many floating-point registers (FPR + FUB)

- **Storage unit (L1D/I cache, cache control unit)**
  - Executes load/store instructions
Enhanced instruction set for the SPARC-V9 instruction set architecture

Extended number of registers
- Floating-point registers are extended the number from 32 to 256
  ➔ Enable to extract parallelism
  ➔ Reduce spill/fill overhead

SIMD operation
- Performs multiple data operation by a single instruction
- Each core executes 2 SIMD operation per clock cycle
  ➔ Each core executes 8 floating-point operations per clock cycle
Software-controllable cache (sector cache)

- Software categorizes the cache data into 2 groups (sectors)
  - For example:
    - sector 0: Less frequently reused data
    - sector 1: Frequently reused data
- Combines the advantages of both the cache and local memory
  - Hardware controls as a cache memory
  - Software can control as a local memory

Other features

- FP Trigonometric functions
- FP Reciprocal Approximation of divide/Square-root
- FP Minimum and Maximum
- Conditional operation

Ex) Sector0:Sector1 = 3:9

L2 Cache structure

```
Way0: 1 1 1 0 0 0 0 0 0 0 0 0
Way1: 1 0 0 1 0 0 0 1 0 0 0 0
```
<table>
<thead>
<tr>
<th>Specification</th>
<th>SPARC64™ VIIIfx</th>
<th>SPARC64™ IXfx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of cores</td>
<td>8 cores</td>
<td>16 cores</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>2 GHz</td>
<td>1.848 GHz</td>
</tr>
<tr>
<td>Cache</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>I: 32KB/core, D: 32KB/core</td>
<td>I: 32KB/core, D: 32KB/core</td>
</tr>
<tr>
<td>L2</td>
<td>6MB (Shared cache)</td>
<td>12MB (Shared cache)</td>
</tr>
<tr>
<td>Peak performance</td>
<td>128 Gigaflops</td>
<td>236.5 Gigaflops</td>
</tr>
<tr>
<td>Memory throughput</td>
<td>64 GB/s</td>
<td>85 GB/s</td>
</tr>
<tr>
<td>Power consumption</td>
<td>58W</td>
<td>110W</td>
</tr>
<tr>
<td>Process</td>
<td>45 nm</td>
<td>40 nm</td>
</tr>
<tr>
<td>Die size</td>
<td>22.7 mm × 22.6 mm</td>
<td>21.9 mm × 22.9 mm</td>
</tr>
<tr>
<td>Number of transistors</td>
<td>Approximately 760 million</td>
<td>Approximately 1.87 billion</td>
</tr>
</tbody>
</table>