MB87M3550
The Fujitsu WiMAX 802.16-2004 SoC

Specification Summary
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# Table of Contents

1. Overview...........................................................................................................................................................................2
   1.1 MB87M3550 Block Diagram ...........................................................................................................................................2
   1.2 Features ...................................................................................................................................................................2

2. Modes of Operation...........................................................................................................................................................4
   2.1 External Processor Mode ............................................................................................................................................4
      2.1.1 Overview.........................................................................................................................................................4
      2.1.2 Local BUS (DSI)..............................................................................................................................................4
      2.1.3 External Processor Responsibilities.....................................................................................................................7
   2.2 Normal Mode ...........................................................................................................................................................7
   2.3 System Application ....................................................................................................................................................7

3. Reference Design................................................................................................................................................................8
   3.1 Hardware Platforms...................................................................................................................................................8
   3.2 Software Platform ...................................................................................................................................................10
      3.2.1 Software Functional Overview...........................................................................................................................11
      3.2.2 Data and Control Interface ........................................................................................................................................12
   3.3 Reference Design Kit ................................................................................................................................................16

4. SoC Top Level Signals and Signal Groups ............................................................................................................................17

5. Operating Conditions and Electrical Specification ................................................................................................................19
   5.1 Digital Characteristics .............................................................................................................................................19
      5.1.1 Absolute Maximum Ratings ...........................................................................................................................................19
      5.1.2 Recommended Operating Conditions .....................................................................................................................19
      5.1.3 DC Characteristics .........................................................................................................................................19
      5.1.4 AC Characteristics and Measurements................................................................................................................19
      5.1.5 Input/Output Pin Capacitance ........................................................................................................................................20

6. Package Mechanical Information .......................................................................................................................................21

7. Supporting Documents.....................................................................................................................................................22
   7.1 Web Access Documents...........................................................................................................................................22
   7.2 Documents for System Development ........................................................................................................................................22

8. Certification and Compliance.............................................................................................................................................24
List of Figures

Figure 1: 1 MB87M3550 SoC System Block Diagram ................................................................. 2
Figure 2: 1 PowerPC DSI Interface .................................................................................................. 5
Figure 3: 1 TDD or HDX FDD Reference Board Evaluation System Using MB87M3550 Internal Processor ................................................................. 8
Figure 3: 2 TDD or HDX FDD Reference Board Evaluation System Using External Processor ................................................................. 9
Figure 3: 3 Full Duplex FDD Reference Board Evaluation System ................................................................. 9
Figure 3: 4 Fujitsu Software Architecture ........................................................................................ 10
Figure 3: 5 MAC Partitioning ........................................................................................................... 11
Figure 3: 6 UMAC-PSAP/LMAC Data and Control Interface Elements ..................................................... 12
Figure 3: 7 Data and Control Sequence for a Typical Transmission [SS] [BS] ................................................................. 13
Figure 3: 8 Base Station Data and Control Sequence for a Typical Reception [BS] ..................................................... 13
Figure 3: 9 Subscriber Station Data and Control Sequence for a Typical Reception [SS] ..................................................... 14
Figure 3: 10 PSAP/LMAC-UMAC Data Interface ......................................................................................... 14
Figure 3: 11 PSAP/LMAC-UMAC Control Interface ......................................................................................... 15
Figure 3: 12 Reference Board Photo ........................................................................................................ 16
Figure 3: 13 What is included in the Reference Kit? ................................................................................. 16
Figure 4: 1 Functional Signal Group Diagram (Internal Processor Mode) ................................................................. 17
Figure 4: 2 Functional Signal Group Diagram (External Processor Mode) ................................................................. 18
Figure 5: 1 Equivalent Circuits for AC Measurements ......................................................................................... 20
Figure 5: 2 AC Measurements .................................................................................................................. 20

List of Tables

Table 2-1 DSI Slave Interface ........................................................................................................... 5
Table 2-2 Memory & External Device Interface ......................................................................................... 6
Table 4-1 Shared Signals for Different Modes of Operation ........................................................................... 18
Table 5-1 Absolute Maximum Ratings ........................................................................................................ 19
Table 5-2 Recommended Operating Conditions ......................................................................................... 19
Table 5-3 DC Characteristics .................................................................................................................. 19
Table 5-4 AC Characteristics Variation ........................................................................................................ 19
Table 5-5 IO Pin Capacitance ................................................................................................................... 20
Table 7-1 NDA Documents ..................................................................................................................... 22
Introduction

With a MAC-to-PHY implementation of the IEEE 802.16-2004 Broadband Wireless Access (BWA) standard, the Fujitsu WiMAX SoC, MB87M3550, offers a cost-effective solution for both subscriber station and base station applications. This highly integrated SoC implements MAC, PHY, radio control, and all the necessary analog circuits for the appropriate 2 to 11GHz licensed or license-exempt bands.

The Fujitsu WiMAX SoC, MB87M3550, fully complies with the IEEE 802.16-2004 standard using an OFDM PHY. The SoC can operate in TDD or FDD modes and supports all the available channel bandwidths from 1.75MHz up to 20MHz. Any desired bandwidth can be implemented by applying the appropriate sampling clock to the SoC. When applying 64QAM modulation in a 20MHz channel and using all 192 sub-carriers, the chip can sustain up to 100Mbps peak data speed. Uplink subchannelization is supported as defined in the IEEE 802.16-2004 standard.

The SoC's integrated UMAC RISC engine implements 802.16 upper layer MAC, scheduler, drivers, protocol stacks, and user application software. A multi-channel DMA controller is responsible for high-speed transactions between various agents on a high performance bus.

The 802.16 Lower Layer MAC functions are implemented in a flexible RISC/DSP engine to off-load Upper layer MAC Processing and to provide performance enhancement. The encryption/decryption engines (AES & DES) are tightly coupled with Lower Layer MAC Processor and are controlled by the physical layer management entity that communicates with the MAC privacy sub-layer to support all security options.
1. Overview

1.1 MB87M3550 Block Diagram
Fujitsu WMAN single chip is designed to enable deployment of a cost effective solution for Customer Premises Equipment (CPE) manufacturers and Subscriber Station (SS) developers of Broadband Wireless Access applications. The chip complies with WIMAX 802.16-2004 standard over the air using a single OFDM PHY in CPE TDD or CPE HDX FDD for up to a 20MHz channel operation. Fujitsu WMAN chip also supports sub-channels in the uplink as defined in 802.16e for mobile applications. The bandwidth can be set to match the configuration of the base-band and IF filters in the external RF section. The reference design allows programming of an external frequency synthesizer to generate the exact sample clock required. The chip implements MAC & Physical (PHY) layer functions and includes analog modules to reduce the total cost of the CPE/SS. A high-level system block diagram is shown in Figure 1:1.

Figure 1:1 MB87M3550 SoC System Block Diagram

Figure 1:1 represents the SoC interface for developing a system with external off-chip components. The SoC interfaces with the following off-chip devices:

1. Clock generation components: VCTCXO, DDS
2. External memory: FLASH, SDRAM
3. RF interface board (for interfacing with a Radio Board)
4. Temperature sensor
5. External mode application processor (example: an external PowerPC-based system)

1.2 Features
- Fully compliant with IEEE 802.16-2004 with the following implementations:
  - OFDM PHY with TDD and HDX FDD.
  - Uses 256-point FFT for broadband transmission.
  - 64QAM, 16QAM, QPSK, BPSK modulation.
  - Uplink subchannelization. Uplink supports 16 subchannels for SS. BS can support 1 subchannel on uplink.
  - MAC PDU CRC.
• DFS using an Rx power detector which is multiplexed into the Power Measurement ADC.
• DES/AES encryption/decryption for 802.16 MAC privacy sublayer.

Baseband IF interface with integrated ADC and DAC
• Output interface is an analog I and Q signal from dual high-speed 10-bit DACs.
• Input interface is an analog I and Q signal to dual high-speed 10-bit ADCs.
• Interpolation/decimation filters with 2x oversampling provide better rejection of out-of-band signals. Simpler baseband filters are required external to the chip.

Automatic frequency control (AFC) with integrated DAC
• The integrated AFC DAC provides control voltage for adjusting external VCTCXO. The DAC is controlled by a hardware control register and has 12-bit resolution for ±10 ppm VCTCXO.

Transmit and receive power measurement with integrated ADC
• Analog input of ADC is connected to an external power detector to sample the transmit (Tx) power. This port can alternately switch to sample another analog level from a receive (Rx) power detector in support of Dynamic Frequency Selection. An integrated switch is provided to multiplex different sources to the ADC.

RF attenuator control
• Programmable Rx AGC for supporting broad range of RF attenuators.

Integrated ARM-926 RISC Processor
• RM-926 RISC Processor running at 160MHz CPU speed, 16K I-Cache, 4K D-Cache.
• Most of Layer 2, 802.16 Upper MAC and Layer 3+ functions are implemented in software running on ARM.

Integrated ARC-Tangent RISC processor
• ARC-4 RISC Processor running at 160MHz, 64Kbyte Code RAM, and 32Kbyte LD/ST RAM, and 16Kbyte of Scratch Pad memory
• Implements Lower 802.16 MAC

• DES engine, AES engine, CRC, and CID Search are implemented in hardware (in ARC-4 Sub-System) and can be invoked by an instruction extension.

Integrated memory controller
• SDRAM controller for up to 64 Mbytes.
• FLASH interface. The external FLASH memory is initially mapped to the beginning of memory for start of program execution. FLASH size is up to 32 Mbytes.
• Generic bus interface for external peripherals.

Integrated general purpose DMA controller
• Supports 4-channel, linked transfer (chaining), descriptor based, and burst transfer.

Integrated Ethernet MAC and DMA
• Ethernet 10/100 MAC & DMA controller with an MII interface for the external Ethernet PHY. The DMA Controller can support scatter-gather for the fragmented Tx data and byte-aligned Tx/Rx packet buffer.

Integrated peripherals:
• Integrated UART/RS-232 interface for general-purpose diagnostic and configuration.
• I²C interface for accessing a temperature sensor or EEPROM in the RF section.
• SPI interface to control external peripherals such as the DDS for clock programming.
• Configurable 25-pin GPIO from UMAC processor for control of and data collection from the RF section of the system. Configurable 4-pin GPIO from LMAC processor.
• Two independent debug ports for both LMAC and UMAC processors.

Integrated programmable PLLs to support multiple frequencies for UMAC, LMAC and baseband processor subsystems
• 0.18μ technology, 1.8 V core, 3.3 V I/O
• JTAG interface
• 436 FDH BGA package (Lead-free and RoHS Compliant)
2. Modes of Operation

The CMODE (chip mode) pin allows the MB87M3550 chip to be used in internal mode (CMODE = 0) or external mode (CMODE = 1) applications. The difference between internal and external application is the MAC processor. For internal mode application, the UMAC processor is used to run the 802.16-2004 Upper MAC. For external mode application, a high-performance external processor is used instead of the UMAC processor. Both modes will support subscriber station (SS) or base station (BS) applications; however, when external mode is used a high-performance processor can replace the on-chip UMAC processor subsystem for applications that demand more computing power such as carrier-class base stations.

2.1 External Processor Mode

2.1.1 Overview

CMODE is set to 1 for this mode. In this mode, the UMAC CPU and subsystem are disabled. An external Upper MAC processor is connected to the Direct Slave Interface (DSI) of the MB87M3550 chip. With DSI, the external processor is the master and the MB87M3550 chip is the slave. The physical pins of the DSI signals are shared with the external memory bus as it is disabled in external processor mode. In this application, the 802.16 Upper MAC runs on a more powerful processor. The LMAC processor runs the Lower MAC time critical functions.

In case of full-duplex FDD, two MB87M3550 chips are required with two separate DSI data paths; one is for transmit and the other one for receive providing a full-duplex application. The DSI connects to the Code RAM and LD/ST interfaces of the LMAC processor. The LMAC processor in the transmit path will be executing transmit software and the one in the receive path will be executing receive software. Similarly, each PHY will be handling either a transmit or a receive function. On the transmit path, the external MAC processor sends PDUs into the LMAC processor. The LMAC processor processes the data and sends it to the PHY. On the receive path, receive data from the PHY is sent to the LMAC and then to the UMAC processor (which could be on-chip or off-chip).

2.1.2 Local BUS (DSI)

Direct Slave Interface (DSI) is a synchronous interface, and it can be connected to a bus interface running at a different clock frequency from the LMAC processor bus. The LMAC processor bus runs at 160MHz; for optimum data transfer, the external processor bus should run at a multiple of 80MHz. With bus systems greater than 80MHz, a bus clock divider reduces the bus clock feeding into the DSI. For example, a bus running at 160MHz will require a divide-by-2 clock divider. Synchronizing logic synchronizes the external processor data transfer at the beginning of the DSI clock cycle and also generates wait signals to extend data latency over the DSI clock cycle. Details of this interface are given in Chapter 4 of the MB87M3550 Datasheet.

2.1.2.1 DSI Interface Description

The DSI Interface with PowerPC is as shown in Figure 2:1. It uses the UPM (User Programmable Machine) of the Local Bus Controller of MPC8560 QuickIII processor. The User Programmable Machine is a flexible interface that can connect to a wide range of devices. The UPM has an internal RAM array that specifies the logical value driven on the control signals for a given clock cycle. Each word in the RAM array provides bits that allow a memory access to be controlled with a resolution of up to one quarter of the external bus clock period on the byte-select and chip-select lines. The LBCLK is divided by programming the LCRR [CLKDIV] field of PowerPC. DSI_CLK frequency is 80MHz.

The DSI Slave side interface is similar a Synchronous SSRAM interface giving the host single or burst accesses of eight beats. The combination of Byte Enables and the Address lines [1:0] will decide whether it is a byte, halfword, or word access. For byte or halfword accesses, the address should be byte aligned or halfword aligned respectively for bursts if the access is in bytes or halfwords. The addresses will then be incremented in bytes or halfwords. See Table 2-1 for valid byte enable combinations. Address [16] = 0 will direct the access to Code RAM otherwise the access goes to LD/ST RAM.

---

Table 2-1: DSI Slave Interface

<table>
<thead>
<tr>
<th>Byte Enables</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>1110</td>
<td>Byte access</td>
</tr>
<tr>
<td>1101</td>
<td></td>
</tr>
<tr>
<td>1011</td>
<td></td>
</tr>
<tr>
<td>0111</td>
<td></td>
</tr>
<tr>
<td>1100</td>
<td>Halfword access</td>
</tr>
<tr>
<td>0011</td>
<td></td>
</tr>
<tr>
<td>0000</td>
<td>Word access</td>
</tr>
<tr>
<td>Any other combination</td>
<td>Word access</td>
</tr>
</tbody>
</table>
### 2.1.2.2 DSI Pins

#### Table 2-2 Memory & External Device Interface

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Drive</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>External Processor Mode:</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LB_BE#[3:0]</td>
<td>I/O</td>
<td>4mA</td>
<td><strong>Local Bus Byte Enables (Inputs).</strong> One bit per byte is used to indicate a valid data byte for host Read/Write accesses.</td>
</tr>
<tr>
<td>ECS#[5] = LB_CS#</td>
<td>I/O</td>
<td>4mA</td>
<td><strong>LB_CS# (Input):</strong> Local Bus Chip Select. The Local Bus (DSI) is accessed only if “Chip Select” is asserted. Active low signal enables the interface for read/write operation.</td>
</tr>
<tr>
<td>ECS#[4] = LB_RDYMODE</td>
<td>I/O</td>
<td>4mA</td>
<td><strong>LB_RDYMODE (Input):</strong> Local Bus Ready Mode. Ready mode input is used for timing selection of presenting the valid data on the DSI Bus during a read operation after LB_RDY# asserted.</td>
</tr>
<tr>
<td>ECS#[3] reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ECS#[2:0] = LB_SIZE[2:0]</td>
<td></td>
<td></td>
<td><strong>LB_SIZE[2:0] (Input):</strong> Local Bus Burst Size. The bus master asserts these pins to indicate that the current transaction is a burst transaction with variable burst sizes up to a maximum of eight words. Burst transfer can be performed in Byte or Words depending on LB_BE#[3:0] signals. If LB_SIZE[2:0] bits are zero, no burst is initiated.</td>
</tr>
<tr>
<td>LB_W/RD#</td>
<td>I/O</td>
<td>4mA</td>
<td><strong>Local Bus Read/Write Enable (Input).</strong> Active low signal enables read and active high signal enables write operation.</td>
</tr>
<tr>
<td>LB_RDY#</td>
<td>I/O</td>
<td>–</td>
<td><strong>Local Bus Ready (Output).</strong> Upon a read access, this signal is asserted to indicate to the host processor when the data on the data bus is valid. The timing of presenting the valid data on the bus is based on LB_RDYMODE. For a write operation this signal is not used. For detailed timing refer to ARC subsystem description.</td>
</tr>
<tr>
<td>LB_DATA[31:0]</td>
<td>I/O</td>
<td>4mA</td>
<td><strong>Local Bus Data (I/O).</strong> Data bus bits 31-0 for the Local Bus (DSI) interface used by external host processor for data transfer between host and ARC Code RAM &amp; Load/Store RAM. In write transactions, the bus master drives the valid data on this bus. In read transactions, the slave (ARC) drives the valid data on this bus.</td>
</tr>
<tr>
<td>LB_ADDR[16:0]</td>
<td>I/O</td>
<td>4mA</td>
<td><strong>Local Bus Address (Input).</strong> Address bus bits 16-0 for the Local Bus (DSI) interface used by external host processor to access the internal address space of ARC Code RAM (64Kbyte) &amp; Load/Store RAM (32Kbyte). — Input Only.</td>
</tr>
<tr>
<td><strong>External Processor Mode Only:</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LB_CLK</td>
<td>I</td>
<td>–</td>
<td><strong>Local Bus Clock.</strong> This clock is used for synchronous local bus (DSI) transactions between external host processor and ARC local memories. This clock is asynchronous with ARC internal clock and can support a maximum frequency of 80MHz.</td>
</tr>
</tbody>
</table>
2.1.3 External Processor Responsibilities
Since the UMAC CPU and subsystem are disabled, functions
normally handled by the UMAC processor subsystem must be
handled externally. Such functions include those handled by the
following blocks:
- SPI
- I2C
- UMAC GPIO
- Power monitoring ADC
- AFC DAC
- Ethernet MAC

2.2 Normal Mode
CMODE pin is set to 0 for this mode. In this mode, the on-chip
UMAC CPU and its subsystem are used to run the 802.16 Upper
MAC. External processor interface (DSI) is disabled.

2.3 System Application
The MB87M3550 can be used in the following applications:
- BWA systems compliant with WiMAX
  1. Residential CPEs (subscriber stations): Low-cost
     802.16 subscriber stations.
  2. Enterprise CPEs: High-throughput subscriber
     stations where an external MAC processor
     (Upper MAC) can be used to boost performance.
  3. Base stations: For point-to-point or
     point-to-multi-point.
- Licensed and license exempt bands of 2–11GHz
- Independent frequency band suitable for 2.5, 3.5, 3.6 or
  5.8GHz
- Half FDD/full FDD or TDD applications

For full-duplex FDD applications two chips are required. For
higher performance and more demanding base stations, an external
processor can be used.

Complete reference designs are available for various purposes. The
process toward certification by the WiMAX Forum is underway for
the full-system version. This reference design includes all the
software and hardware required for a cost-effective system solution.

2. Refer to “MB87M3550 Application Guide” and “MB87M3550 SoC
Reference Kit Manual” documents for system applications.
3. Reference Design

3.1 Hardware Platforms
Several hardware platforms are available with options for performing chip, software, and system verification. The Reference Board evaluation system for subscriber stations (Figure 3:1) can be configured to support either TDD or HDX FDD, depending on the radio selection.

This configuration can be suitable Subscriber Station TDD or HDX FDD applications.

Figure 3:2 provides an example of Reference Board configuration using an external processor. The simplified base station evaluation system of Figure 3:3 provides an example of a full duplex FDD implementation using an external processor.

The key features of the evaluation boards include:
- RF port interface for third-party radio
- Radio module
- Network interface
- On-board memory
- On-board control using SPI, I2C, and GPIO
- Debug port interfaces
- RS-232C interface port
- External power supply interface

Figure 3:1 TDD or HDX FDD Reference Board Evaluation System Using MB87M3550 Internal Processor

This configuration can be suitable for subscriber station TDD or HDX FDD applications.
This configuration can be SS or BS for TDD or HDX FDD applications.

Figure 3:2 TDD or HDX FDD Reference Board Evaluation System using External Processor

This configuration can be suitable for base station and backhaul applications.

Figure 3:3 Example of a Full Duplex FDD Implementation
3.2 Software Platform
The Fujitsu 802.16 software platform implements a subscriber station or base station with the following features:

- Compliance with IEEE 802.16-2004 standard specification
- MAC security sublayer for subscriber station authentication and data encryption
- Multiple service class support to differentiate service quality
- Dynamic service management to activate service class when needed
- MAC portability to different RTOSs

The typical 802.16 software platform available from Fujitsu contains the following components:

- Host software (runs on either the on-chip UMAC or external processor) with the following subcomponents:
  1. Board support packages (BSPs) for popular operating systems
  2. RTOS wrapper
  3. Device drivers, such as Ethernet, IIC, SPI, UART, etc.
  4. BS or SS management and application
  5. 802.16 upper layer MAC
- 802.16 PHY service access point and lower layer MAC (PSAP/LMAC) firmware (runs on the on-chip LMAC processor)

As shown in an overview of Fujitsu’s software platform (Figure 3:4), the 802.16 upper layer MAC accesses the OFDM PHY through PSAP/LMAC firmware running on the on-chip LMAC processor. In addition to providing PHY access primitives, the PSAP/LMAC firmware includes some 802.16 lower layer MAC functionality to offload tasks from the upper layer MAC. This functionality includes encryption/decryption engines and a CRC checker/inserter.

Fujitsu provides the BSP and device drivers for the supported operating systems, as well as the RTOS wrapper, thus simplifying the porting of the complete software suite to any operating system supported by Fujitsu. Fujitsu’s 802.16 upper layer MAC can also be replaced with a third-party component. Fujitsu provides full API and interface specifications to enable third parties to develop upper layer MAC components.

Fujitsu also provides the PSAP/LMAC firmware for BS and SS applications. The upper layer MAC coupled with the PSAP/LMAC firmware make up the complete 802.16 protocol stack.
3.2.1 Software Functional Overview

The following Figure shows major tasks implemented in Upper MAC (UMAC) and in Lower MAC (LMAC):

A brief overview of PSAP/LMAC is provided in the following sub-sections. Details of PSAP/LMAC can be found in the Fujitsu MB87M3550 PHY Service Access (LMAC) Specification. This specification has been developed to support UMAC development.

The PSAP/LMAC has 3 main operational modes: **IDLE**, **SCAN** and **RUN**. Each of these modes is briefly explained in the following sections. Note: In the description that follows, [SS] implies that the description applies to Subscriber Station only, [BS] implies that the description applies to Base Station only, and [SS][BS] imply that the description applies to both SS, and BS.

### 3.2.1.1 IDLE Mode [SS] [BS]

IDLE is the first mode automatically entered right after the startup. Upon boot-up the PSAP/LMAC initializes and starts waiting in the IDLE mode. The PSAP/LMAC sends a message (through the messaging system) to the UMAC to indicate the arrival at the IDLE mode. In the IDLE mode, PSAP/LMAC does not pass traffic. It only processes messages sent by the UMAC through the messaging system. Messaging System is explained in more detail in the Fujitsu MB87M3550 PHY Service Access (LMAC) Specification.

### 3.2.1.2 SCAN Mode [SS]

The SCAN mode exists only for SS operation and it is for initial synchronization to a BS. The information is provided by the PSAP/LMAC to the UMAC during the SCAN mode to support the initial network entry process. The PSAP/LMAC can be put in the SCAN mode by the UMAC using a mode change message, through the messaging system. Before starting the SCAN mode, the UMAC can optionally initialize various parameters, such as CP length, frame length, etc., if known, via messages sent through the messaging system. In SCAN mode, an attempt to locate and synchronize with a service is made. During the SCAN mode, PSAP/LMAC continuously sends status indicators and data to the UMAC, to support the initial ranging process running on the UMAC. Upon successfully locating and synchronizing to a service, the PSAP/LMAC has to be switched to the RUN mode by the UMAC using a mode change message. This not only terminates the SCAN mode but also starts the RUN mode, where full data traffic is delivered by PSAP/LMAC in both directions. The SCAN mode is not available for BS operation [BS].
3.2.1.3 RUN Mode [SS] [BS]
This is the normal operating mode for the PSAP/LMAC. In the RUN mode, the PSAP/LMAC actually transfers traffic between the UMAC and the OFDM PHY. The RUN mode can be terminated by the UMAC by a mode change message, putting the PSAP/LMAC into either the IDLE mode or the SCAN mode again. In SS, RUN mode can be entered only after a successful SCAN mode completion and upon a mode change message from the UMAC [SS]. In BS, the SCAN mode does not exist and the UMAC must switch the PSAP/LMAC to RUN mode from the IDLE mode by a mode change message [BS].

3.2.2 Data and Control Interface
The data and control exchange between the UMAC and the PSAP/LMAC is handled through separate flows. The traffic burst data and associated control flow utilizes several buffers and data structures allocated in the shared memory section. These flows are explained in detail in the “PHY Service Access Point (LMAC) Interface Specification”. The non-traffic communication between the UMAC and the PSAP/LMAC use a special messaging scheme. The special messaging system is considered as a part of control interface and explained thoroughly in the “PHY Service Access Point (LMAC) Interface Specification”. The main elements of the UMAC-PSAP/LMAC interface are shown in Figure 3:6.

![Diagram of UMAC-PSAP/LMAC Data and Control Interface Elements](image)
There are 2 pointers for each circular buffer, as shown in Figure 3:6, the input pointer (IP) and the output pointer (OP). These pointers are used for data insertion and retrieval from the associated buffer. Whenever new data is to be inserted into a buffer, it is inserted to the location pointed by IP. Similarly, data is retrieved from the location pointed by OP. The following figures show the series of events on data and control interfaces in a typical transmission and reception for BS and SS.

**Figure 3:7 Data and Control Sequence for a Typical Transmission [SS] [BS]**

**Figure 3:8 Base Station Data and Control Sequence for a Typical Reception [BS]**
3.2.2.1 UMAC-PSAP/LMAC Data Interface
The elements constituting the UMAC-PSAP/LMAC data interface are:

- UMAC Transmit Buffer (MAC_TX_BUFFER)
- UMAC Receive Buffer (MAC_RX_BUFFER)
- TX and RX Watermarks
- IPs and OPs to the above buffers
- Watermark Interrupts

The following figure depicts the basic data flow and associated interrupts during typical data flow between the PSAP/LMAC and the UMAC.
There are 2 interrupts associated with the flow of data between the PSAP/LMAC and the UMAC. TX Low Watermark Interrupt is issued by the PSAP/LMAC when the low watermark has been reached in the MAC_TX_BUFFER and the UMAC should write more data to the MAC_TX_BUFFER. RX High Watermark Interrupt is issued by the PSAP/LMAC when the high watermark has been reached in the MAC_RX_BUFFER and the UMAC should collect data from the MAC_RX_BUFFER. Watermark levels can be set by the UMAC using the messaging system.

3.2.2.2 UMAC-PSAP/LMAC Control Interface

The elements constituting the UMAC-PSAP/LMAC control interface are:

- Transmit Control Buffer (TX_CTRL_BUFFER)
- Receive Control Buffer (RX_CTRL_BUFFER) [BS]
- Receive Status Buffer (RX_STAT_BUFFER)
- IPs and OPs to the above buffers

The following figure depicts the basic control flow and associated interrupts during the typical operation of the PSAP/LMAC and the UMAC.

![Figure 3:11 PSAP/LMAC-UMAC Control Interface](image-url)
3.3 Reference Design Kit
The Reference Board is shown in Figure 3:12. Contents of the Reference Kit are shown in Figure 3:13.

The Reference Board of Figure 3:12 shows:

- SS Reference Board with RF board
- BS Reference Board (TDD or FDD) with Power-PC interface and RF board

Figure 3:12 Reference Board Photo

Figure 3:13 What Is Included in the Reference Kit?

- SoC Reference Board
- SoC Baseband Board
- RF Board
- SoC Debugger Board
- Serial Port Cable
- Power Supply
- MCX Cables
- Power Cable
4. SoC Top-Level Signals and Signal Groups

A signal group is shown in Figure 4:1 below for internal processor mode.3

3. See MB87M3550 Datasheet for full description of the signals.
Signals used in external mode are shown in Figure 4:2 below:

**MB87M3550 SOC**

* (External Processor Mode)  

Certain pins of the SoC are shared and have different meanings in external and internal processor modes. Table 4-1 shows pins that are shared for the two modes.

**Table 4-1 Shared Signals for Different Modes of Operation**

<table>
<thead>
<tr>
<th>Internal Processor Mode</th>
<th>External Processor Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECS#[5]</td>
<td>LB_CS#</td>
</tr>
<tr>
<td>ECS#[2:0]</td>
<td>LB_SIZE[2:0]</td>
</tr>
<tr>
<td>EWE[3:0]</td>
<td>LB_BE[3:0]</td>
</tr>
<tr>
<td>EADDR_L[16:0]</td>
<td>LB_ADDR[16:0]</td>
</tr>
<tr>
<td>ECS#[4]</td>
<td>LB_RDONLY</td>
</tr>
<tr>
<td>EREF</td>
<td>LBWRD#</td>
</tr>
<tr>
<td>EREDY</td>
<td>LB_RDONLY</td>
</tr>
<tr>
<td>EDATA[31:0]</td>
<td>LB_DATA[31:0]</td>
</tr>
</tbody>
</table>
5. Operating Conditions and Electrical Specification

5.1 Digital Characteristics

5.1.1 Absolute Maximum Ratings

Table 5-1: Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDI</td>
<td>Internal Core Power Supply Voltage</td>
<td>-0.5 to 2.5</td>
<td>V</td>
</tr>
<tr>
<td>VDDE</td>
<td>External IO Power Supply Voltage</td>
<td>-0.5 to 4.0</td>
<td>V</td>
</tr>
<tr>
<td>VI</td>
<td>Input Voltage</td>
<td>-0.5 to VDDE + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>VO</td>
<td>Output Voltage</td>
<td>-0.5 to VDDE + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>IO</td>
<td>Output Current (Average DC Current)</td>
<td>±4</td>
<td>mA</td>
</tr>
<tr>
<td>Tst</td>
<td>Storage Temperature</td>
<td>-55 to 125</td>
<td>°C</td>
</tr>
<tr>
<td>Tj</td>
<td>Junction Temperature</td>
<td>-40 to 125</td>
<td>°C</td>
</tr>
</tbody>
</table>

The device can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of the absolute maximum ratings.

5.1.2 Recommended Operating Conditions

Table 5-2: Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDI</td>
<td>Internal Power Supply Voltage</td>
<td>1.65</td>
<td>1.8</td>
<td>1.95</td>
<td>V</td>
</tr>
<tr>
<td>VDDE</td>
<td>External IO Power Supply Voltage</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>—</td>
<td>VDDE + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>-0.3</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Tj</td>
<td>Junction Temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

Notes: Recommended operating conditions are normal operating ranges for the device. All the device’s electrical characteristics are guaranteed when operating within these ranges. Always use the device within these recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

5.1.3 DC Characteristics

Measurement Conditions: over recommended operating conditions

Table 5-3: DC Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>VDDE = 3.0</td>
<td>-0.3</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>3.3V Output</td>
<td>2.0</td>
<td>—</td>
<td>VDDE + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>IOL = 100µA</td>
<td>0</td>
<td>—</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>3.3V Output</td>
<td>VDDE = 0.2</td>
<td>—</td>
<td>VDDE</td>
<td>V</td>
</tr>
<tr>
<td>ILI</td>
<td>Input Leakage Current</td>
<td>VDDE = 3.6</td>
<td>—</td>
<td>—</td>
<td>±4</td>
<td>µA</td>
</tr>
<tr>
<td>ICC1</td>
<td>VDDI Supply Current</td>
<td>100MHz Clock</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td></td>
</tr>
<tr>
<td>ICC2</td>
<td>VDDE Supply Current</td>
<td>100MHz Clock</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td></td>
</tr>
<tr>
<td>RP</td>
<td>Pull up/Pull down Resistor</td>
<td>10</td>
<td>33</td>
<td>80</td>
<td>kΩ</td>
<td></td>
</tr>
</tbody>
</table>

5.1.4 AC Characteristics and Measurements

AC characteristics are determined based on junction temperature, supply voltage, and process variations. Table 5-4 shows the variation of AC characteristics under the recommended operating conditions.

Table 5-4: AC Characteristics Variation

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Conditions</th>
<th>Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>tpd(max)</td>
<td>$T_j = 125^\circ C$, VDDI = 1.65 V, VDDE = 3.0 V</td>
<td>$t_{typ} \times 1.58$</td>
</tr>
<tr>
<td>tpd(typ)</td>
<td>$T_j = 25^\circ C$, VDDI = 1.80 V, VDDE = 3.3 V</td>
<td>$t_{typ} \times 1.00$</td>
</tr>
<tr>
<td>tpd(min)</td>
<td>$T_j = -40^\circ C$, VDDI = 1.95 V, VDDE = 3.6 V</td>
<td>$t_{typ} \times 0.64$</td>
</tr>
</tbody>
</table>
The measurements are performed with load capacitance of 30 pF. The equivalent buffer circuit is given in Figure 6:1. The AC measurement parameters are shown in Figure 6:2 with following conditions:

<table>
<thead>
<tr>
<th>Measurement</th>
<th>SW1</th>
<th>SW2</th>
</tr>
</thead>
<tbody>
<tr>
<td>L → H, H → L</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>L → Z, Z → L</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>H → Z, Z → H</td>
<td>OFF</td>
<td>ON</td>
</tr>
</tbody>
</table>

![Figure 5:1 Equivalent Circuits for AC Measurements](image)

![Figure 5:2 AC Measurements](image)

### 5.1.5 Input/Output Pin Capacitance
Input/output pin capacitance is given in Table 6-5.

The measurement conditions are:

$T_j = 25^\circ C, VDD = VIL = 0 V, f = 1 MHz.$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Conditions</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input Pin</td>
<td>16</td>
<td>pF</td>
</tr>
<tr>
<td>COUT</td>
<td>Output Pin</td>
<td>16</td>
<td>pF</td>
</tr>
<tr>
<td>CI/O</td>
<td>I/O Pin</td>
<td>16</td>
<td>pF</td>
</tr>
</tbody>
</table>
6. Package Mechanical Information

436 Face Down Heat-Spreader Ball Grid Array Package (436 FDHBGA). Note: The SoC will use lead free package and is RoHS compliant.

**BGA-436P-M03**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Ball pitch</strong></td>
<td>1.00 mm</td>
</tr>
<tr>
<td><strong>Package width × package length</strong></td>
<td>35.00 × 35.00 mm</td>
</tr>
<tr>
<td><strong>Lead shape</strong></td>
<td>Soldering ball</td>
</tr>
<tr>
<td><strong>Sealing method</strong></td>
<td>Plastic mold</td>
</tr>
<tr>
<td><strong>Ball size</strong></td>
<td>Ø0.60 mm</td>
</tr>
<tr>
<td><strong>Mounting height</strong></td>
<td>1.50 mm MAX</td>
</tr>
<tr>
<td><strong>Weight</strong></td>
<td>4.50 g</td>
</tr>
</tbody>
</table>

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7. Supporting Documents

The following documents have been developed to support systems based on the MB87M3550 SoC. Note that many of these documents require an NDA.

7.1 Web Access Documents
The following Web site is a good resource for initial documents:

- Product Fact Sheet/Product Brief
- Presentation
- White papers
- Press releases
- Documentation
- FAQ

7.2 Documents for System Development
The following documents have been developed to support systems based on MB87M3550 SoC.

Table 7:1 NDA Documents

<table>
<thead>
<tr>
<th>Document Number</th>
<th>Document Title</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>FUJITSU WIMAX SOC Presentation</td>
<td>NDA</td>
<td>Introduction to FUJITSU WIMAX 802.16-2004 SoC.</td>
</tr>
<tr>
<td>01</td>
<td>Fujitsu WIMAX 802.16-2004 SoC MB87M3550 Datasheet</td>
<td>NDA</td>
<td>Introduction, Detailed Features, Pin Description, Description of Internal Sub-systems (Block Diagrams, Memory Map, Register Map Timing Diagrams), Description of Clocks, Power Monitoring, Description of RF interface ADC/DAC, Electrical Characteristics.</td>
</tr>
<tr>
<td>02</td>
<td>Fujitsu WIMAX 802.16-2004 SoC MB87M3550 Programming Guide</td>
<td>NDA</td>
<td>Introduction to MB87M3550 Software Components, functional description of Software modules, partitioning of MB87M3550 Software into Upper MAC (UMAC) and Lower MAC (PSAP) components. Note: PSAP → PHY Service Access Point and there is a separate document that describes PSAP in detail.</td>
</tr>
<tr>
<td>03</td>
<td>Fujitsu WIMAX 802.16-2004 SoC MB87M3550 PHY Service Access Point (PSAP)</td>
<td>NDA</td>
<td>Details for UMAC developer to interface with Fujitsu’s embedded PSAP/LMAC. Description of PSAP/LMAC functions, Description of data and control structures, description of operating modes, network entry and typical operation</td>
</tr>
<tr>
<td>04</td>
<td>Fujitsu WIMAX 802.16-2004 SoC MB87M3550 Application Guide</td>
<td>NDA</td>
<td>Application notes and guidelines containing details of how to use MB87M3550 at the system level, describes system bandwidth, clock, DDS, Sampling Frequency requirements, describes system memory interface for FLASH, SDRAM, Describes internal and external modes (with PowerPC example), contains details of Radio Interface, AGC, AFC, examples of VOIP, T1/E1 applications, contains answers to a number of Frequently Asked Questions (FAQ), Test results and performance data (from SUI Channel model simulations and RF Performance tests for BPSK, QPSK, QAM-16 and 64-QAM).</td>
</tr>
<tr>
<td>05</td>
<td>Fujitsu WIMAX 802.16-2004 MB87M3550 SoC Reference Kit</td>
<td>NDA</td>
<td>The document describes the necessary Hardware and Software components to develop a cost effective, fixed Broadband Wireless Access (BWA) system solution for Subscriber Station (low-cost), Enterprise SS, and Base Stations.</td>
</tr>
</tbody>
</table>
| 06              | SiGe Radio Documentation | NDA | • RF chipset datasheet  
- RF board specification  
- Schematics, layout guide and BOM  
- Performance data  
Note: RF chip technical support will be provided from RF chip companies, not from Fujitsu. Contact information will be provided separately. |
| 07              | PowerPC MPC8550 Documentation | NDA | • Hardware reference manual  
- Schematics and BOM |
After an NDA is in place, the following documents may be provided from the above list:

- Fujitsu WiMAX SoC presentation (Document #00)
- The Fujitsu WiMAX 802.16-2004 SoC Datasheet (Document #01)
- The Fujitsu WiMAX 802.16-2004 SoC Programming Guide (Document #02)

Following information will only be provided to enable customers to make business decision on Fujitsu.

- The Fujitsu WiMAX 802.16-2004 SoC PHY Service access Point (LMAC) Interface Specification for UMAC Developers* (Document #03)
- The Fujitsu WiMAX 802.16-2004 SoC Application Guide (Document #04)
- The Fujitsu WiMAX 802.16-2004 SoC Reference Kit (Document #05)
- SiGe RF board Documentation (Document #06)
- PowerPC MPC8560 Board Documentation (Document #07)

*Only for customers who develop their own upper MAC.
8 Certification and Compliance

Fujitsu has designed the MB87M3550 wireless MAN SoC to comply with the IEEE 802.16-2004 standard and intends to certify systems according to WiMAX profiles.

For more information
More information on the IEEE 802.16 standard for broadband wireless access and the WiMAX Forum is available at www.wimaxforum.org and www.ieee802.org/16.

For more information on Fujitsu's broadband wireless SoC, please address e-mail to inquiry.bwa@fma.fujitsu.com.

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Revision History:

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<td>7/12/06</td>
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<td>Release 1.0</td>
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