

MB87Q2020
40G Forward Error Correction Device

February 2004
Version 1.0

Overview

The MB87Q2020 is a multi-rate multiple forward error correction code device supporting Sonet/SDH, OTN and ClearChannel signals. The device can be configured in transceiver and regenerator modes at 40/43 Gbit/s data rates.

In transceiver mode either a constant bit rate 40Gbit/s signal (CBR-40G) (Sonet/SDH or clear channel) or an OTU-3 signal can be mapped into a line side G.709/798 compliant transmission format (add functionality). Simultaneously a G.709/798 compliant client signal or a CBR-40G client signal can be extracted from an incoming G.709/798 compliant line signal (drop functionality). Add and drop functionality can be operated independently. For Sonet/SDH client signals reduced receive and transmit byte processing according to ITU-T G.707/ANSI T1.105 is supported.

In regenerator mode the MB87Q2020 provides full G.709/798 compliant byte processing with the following FEC converter options:

FEC repeater mode:

RS decoding, RS re-encoding or UFEC decoding, UFEC re-encoding

FEC translator mode:

UFEC decoding, RS encoding or RS decoding, UFEC encoding

Features

Forward Error Correction

- ITU-T G.975 & G.709 compliant Reed-Solomon code
- G.709V compliant proprietary ULTRA FEC code
 - Additional 2 dB gain vs. standard RS code at BER=1e-16
 - Greater than 8 dB of net electrical coding gain at 1e-16
 - Converts an input BER 1e-3 to an output BER < 1e-17
 - Flags uncorrectable code words
 - entire chip latency < 6µs
- Low power design
- Extensive bit error statistics
 - BER monitors for FEC
 - Uncorrectable blocks
- Bypass capabilities for FEC

OTN processing features

- OTU-3 overhead processing according to ITU-T G.709/798
- Synchronous and asynchronous mapping of single client signals into OTU-3/OTU-3V frames
- Two types of forward error correction codes with 7% overhead
 - Proprietary ULTRA FEC (UFEC)
 - Standardized Reed-Solomon RS(255,239) code
- FEC bypass function for non-intrusive monitoring purposes
- Provisionable generic AIS detection & insertion on client side
- Internal Backward Indication Channel (BIC)
- Internal and external Overhead Access Channel (OAC)

Sonet/SDH features

- ITU-T G.707/ANSI T1.105 compliant Sonet/SDH overhead processing
- Optical Section termination features
 - LOS detection
- Optical Section / Regenerator section adaptation features
 - A1 / A2 framing
 - Scrambling/Descrambling
- Regenerator section features
 - B1 performance monitoring (block error, bit error)
 - J0 persistency check, extraction, mismatch detection (1/16/64 bytes)
 - Generic AIS detection (error tolerant) & generation

Network test features

- PRBS pattern generators
- Error generators for FEC testing
- Bit error rate tester
- Configurable framing algorithm
- 'walking -one' interface test
- dedicated high-speed outputs for internal control signals

Technology and Package

- 0.11 um CMOS Technology (0.095um, Ldrawn)
- 1.2 V / 2.5 V power supply
- 900 pin FC-BGA
- Total power consumption < 10 W

Applications

- Ultra long haul
 - Add functionality with optional G.707/ANSI T1.105 compliant receive / transmit byte processing (reduced RST) and G.709/798 compliant RS FEC / ULTRA FEC (OTU-3V mapping)
 - Drop functionality with optional G.707/ANSI T1.105 compliant receive / transmit byte processing (reduced RST) and G.709/798 compliant RS FEC / ULTRA FEC (OTU-3V demapping)
 - FEC converter (G.709/798 compliant)
 - decode ULTRA FEC (OTU-3V) and encode with standardized RS FEC (OTU-3)
 - decode RS FEC (OTU-3) and encode with proprietary ULTRA FEC (OTU-3V)
- Standard OTN
 - Add functionality with optional G.707/ANSI T1.105 compliant receive / transmit byte processing (reduced RST) and G.709/798 compliant RS FEC / ULTRA FEC (OTU-3/3V mapping)
 - Drop functionality with optional G.707/ANSI T1.105 compliant receive / transmit byte processing (reduced RST) and G.709/798 compliant RS FEC / ULTRA FEC (OTU-3V demapping)
 - Regenerator (through) functionality with G.709/798 compliant RS FEC / ULTRA FEC
- Network test set
 - Programmable bit error generators and monitoring
 - Programmable data generators

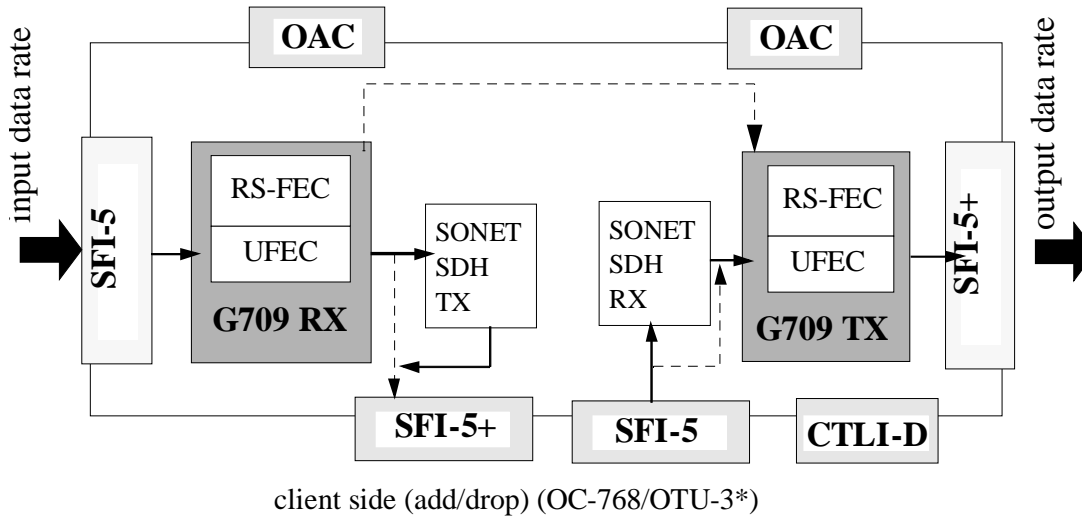
Interfaces

- SFI-5 (OIF2001-145.10) compliant line interface
 - 16 bit + deskew @ 2.5/2.7 Gbit/s
 - CML interface level
- SFI-5 (OIF2001-145.10) compliant client interface
 - 16 bit + deskew @ 2.5/2.7 Gbit/s
 - CML interface level
- Overhead Access Channel
 - Full Och overhead access via serial interface
- CPU interface
- GPIO
 - General purpose interfaces for dedicated board control
- IEEE-1149.1 JTAG port
 - Memory bist, boundary scan

Board Design Support

- Bus reversal (Data)
- Bit inversion (Data, Deskew)
- Deskew alignment
- Supports bit-/bytestripping

Functional block diagram



note: OTU-3*: OTU-3 compliant frame format, FEC is not processed

Ultra-FEC Coding Gain

