

# 1M-bit (×8/×16) FRAM<sup>®</sup>

## MB85R1001/MB85R1002

This products is a FRAM<sup>®</sup> of 1M-bit 1T1C cell design, featuring high-density, low-power consumption, and high-performance of write/read operation times.

### Introduction

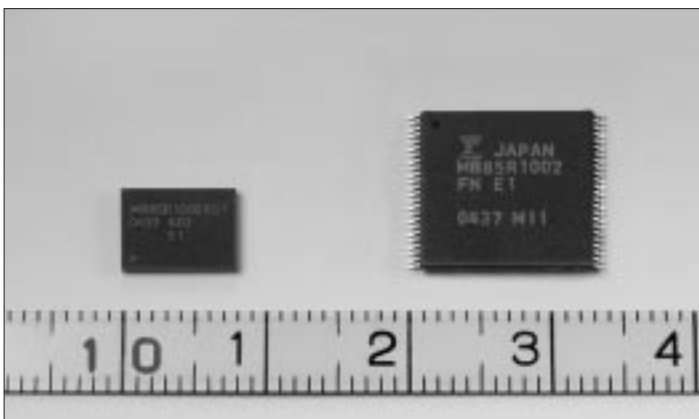
Non-volatile ferroelectric random access memory (FRAM) features a high-speed read/write operation and low power consumption and it is used not only as a single memory chip but is also packaged with several other FRAM devices to provide a microcomputer product. The total shipment of FRAMs from FUJITSU has reached 160 million since the start of their mass production. FUJITSU has now developed a new series FRAM of 1T1C cell design that offers a density of 1M-bit, the largest among FUJITSU's FRAM products.

### Product Features

#### ■ Chip Configuration

- MB85R1001: 128K words×8-bit configuration
- MB85R1002: 64K words×16-bit configuration

Photo 1 External View



#### ■ Operating Conditions

- Supply voltage: +3.0V to +3.6V (No need for 12V or other higher voltage)
- Operating temperature range: -20°C to +85°C
- Read access time: 100ns
- Read cycle time/Write cycle time: 250ns

#### ■ Circuit Functions

- ECC (Error Correcting Code) circuit
- /LB and /UB data byte control (MB85R1002)
- Power-on protect function

#### ■ Package

- 48-pin TSOP package
- 48-pin FBGA package (MB85R1002)

Photo 2 Chip



**Table 1** lists the principal characteristics, **Figs.1** and **2** show pin assignments, **Fig.3** depicts the block diagram, **Fig.4** provides the dependence of access time on power-supply voltage, **Table 2** lists the operation modes available with MB85R1002, and **Fig.5** shows the read cycle time.

## Product Functions

MB85R1002 allows 8-bit byte access for both lower and upper digits with the aid of data bus control terminals /LB and /UB. The package is available in TSOP-48 and FBGA-48.

- TSOP-48: Outside dimensions 12mm×12.4mm  
Lead pitch 0.50mm
- FBGA-48: Outside dimensions 8.1mm×6.1mm  
Lead pitch 0.75mm

This new product also provides /OE control and /WE control cycles as a pseudo SRAM mode.

## Future Development

FUJITSU will continue to implement further highly integrated design based on 0.18 $\mu$ m process technology, aiming for higher density and lower voltage operation, as the leading company

providing FRAM products. Based on its technologies, FUJITSU is supplying FRAM chips to the market that can take full advantage of high-speed and non-volatile features. \*

### NOTES

\*FRAM is a registered trademark of Ramtron International Corporation.

**Table 1** Principal Characteristics

Chip name		MB85R1001	MB85R1002
Chip configuration		128K words×8-bit	64K words×16-bit
Read cycle time	tRC	250ns	
Write cycle time	tWC	250ns	
CEB access time	tCE	100ns	
Operating current	ICC	1.5mA@1MHz	

**Table 2** Operation Modes available with MB85R1002 (×16)

Mode	/CE1	CE2	/OE	/WE	/LB	/UB	I/O<1:8>	I/O<9:16>
Stand-by	H	X	X	X	X	X	High-Z	High-Z
	X	X	X	X	H	H	High-Z	High-Z
	X	X	H	H	X	X	High-Z	High-Z
	X	L	X	X	X	X	High-Z	High-Z
Read	H → L	H	L	H	L	L	Dout	Dout
					L	H	Dout	High-Z
					H	L	High-Z	Dout
Read (Pseudo SRAM, /OE control)	L	H	H → L	H	L	L	Dout	Dout
					L	H	Dout	High-Z
					H	L	High-Z	Dout
Write	H → L	H	X	L	L	L	Din	Din
					L	H	Din	High-Z
					H	L	High-Z	Din
Write (Pseudo SRAM, /WE control)	L	H	H	H → L	L	L	Din	Din
					L	H	Din	High-Z
					H	L	High-Z	Din

Figure 1 MB85R1002 Pin Assignments (TSOP-48)

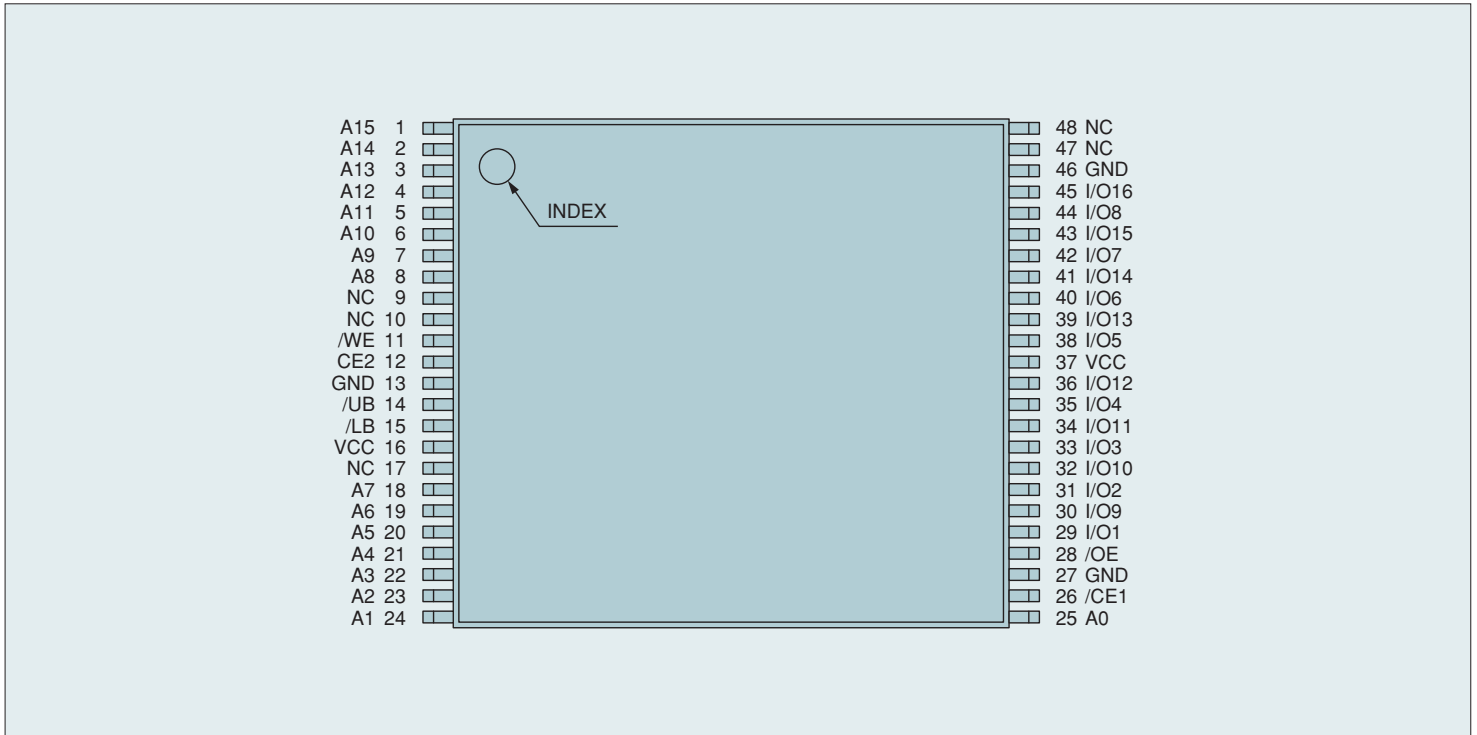


Figure 2 MB85R1002 Pin Assignments (FBGA-48)

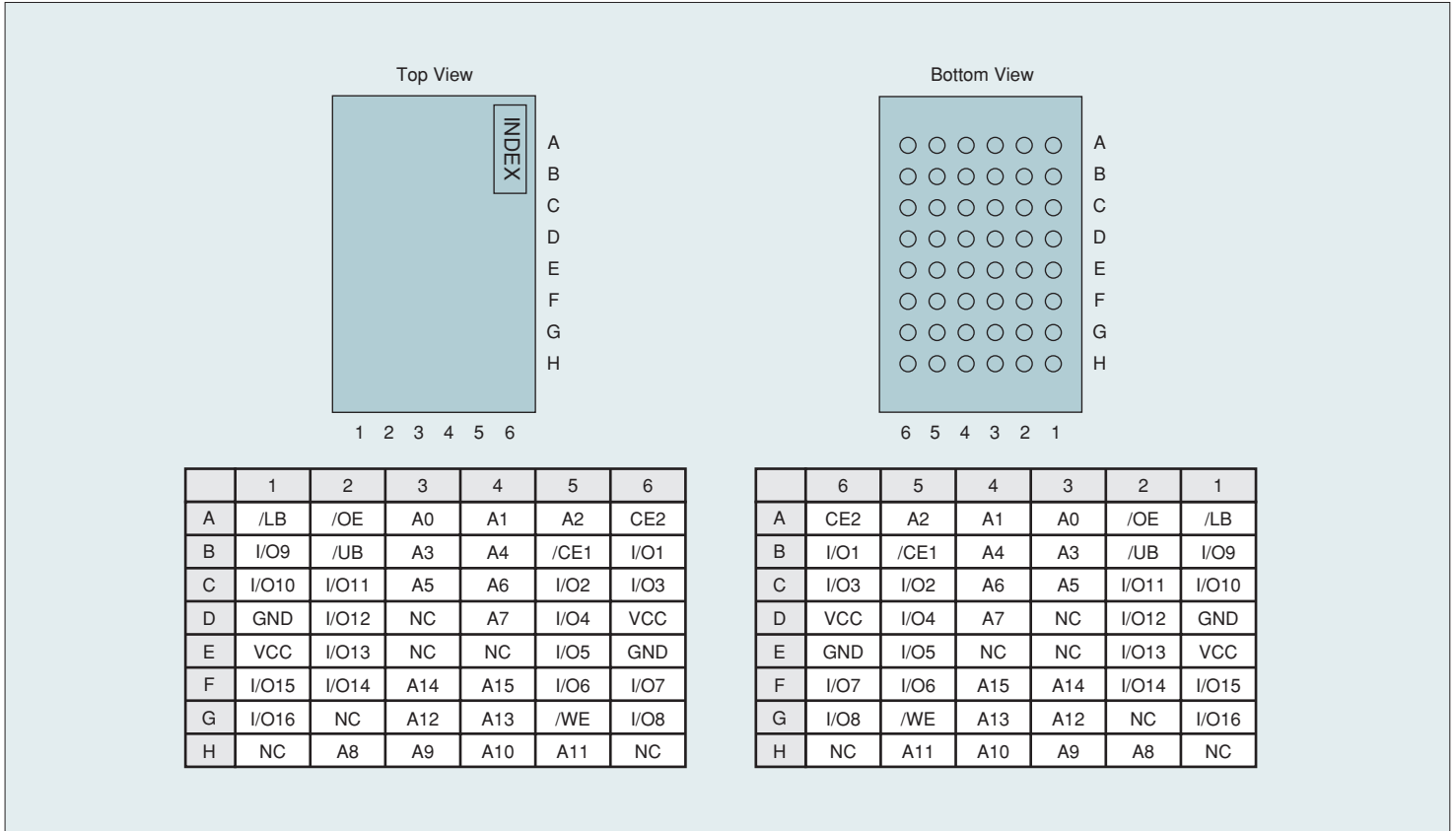


Figure 3 MB85R1002 Block Diagram

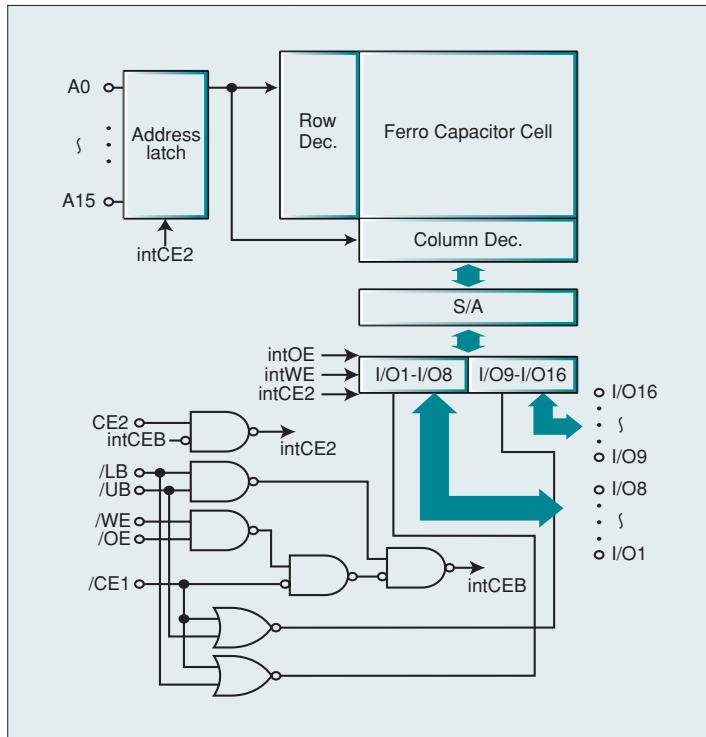


Figure 4 Dependence of Access Time on Power Supply Voltage

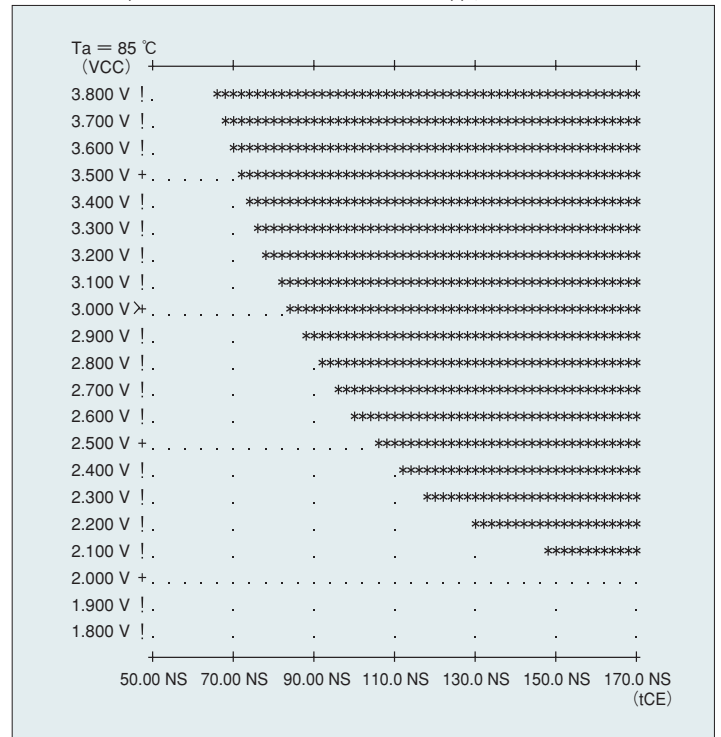


Figure 5 Read Cycle Time

