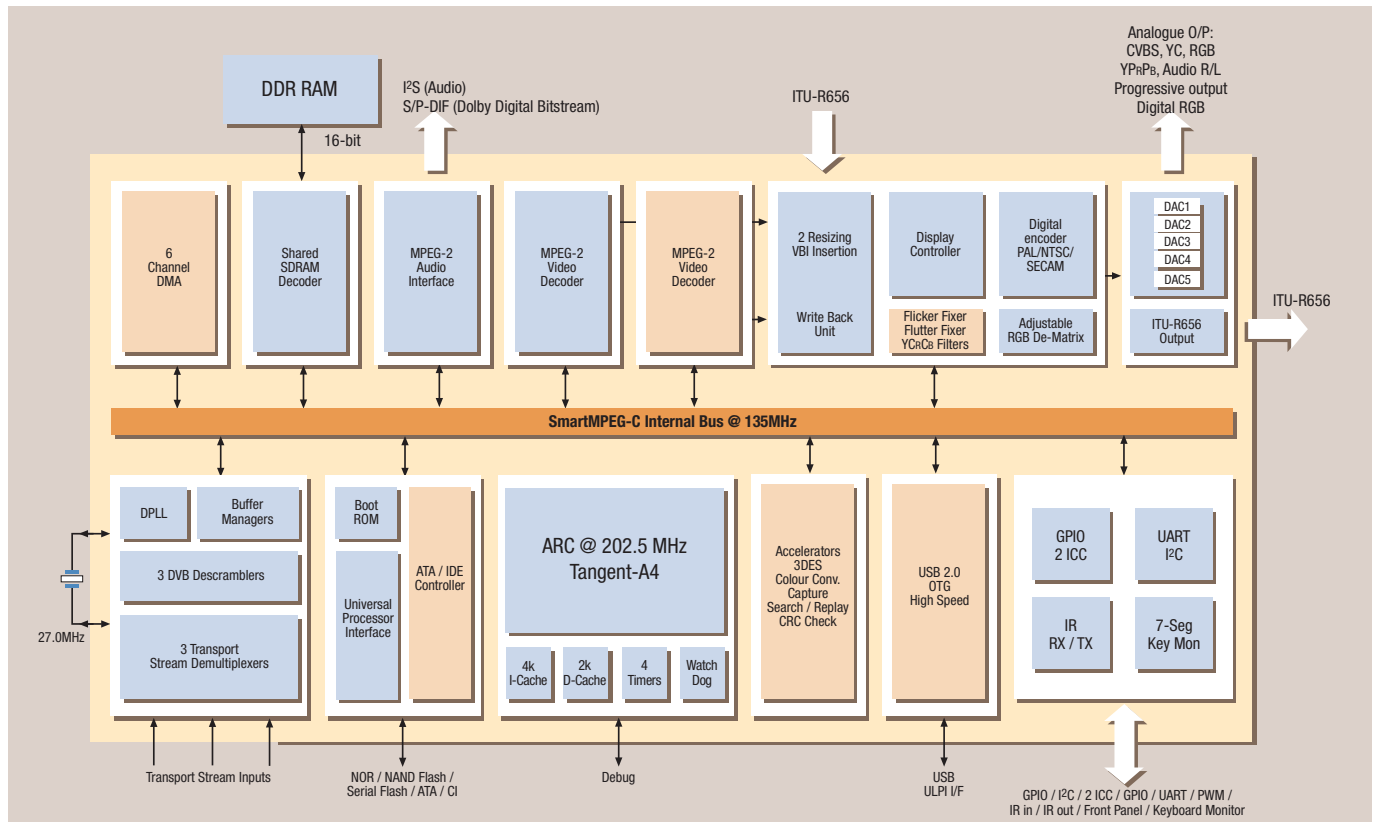


# MB86H35

SmartMPEG-C

## Digital TV decoder for STBs and PVRs



MB86H35 SmartMPEG-C block diagram.

### Description

The SmartMPEG-C is an advanced digital television decoder designed to meet the needs of tomorrow's set-top box and IDTV markets. The SmartMPEG-C includes advanced features to support personal video recorder (PVR) applications including two video decoders, hardware DMA, and encryption. It also includes an LCD output channel to enable simple connection to an LCD panel and HDMI transmitter.

A 202.5MHz ARC Tangent-A4 CPU with a 2kByte data and 4kByte instruction cache is included. The CPU is connected to a shared 16-bit DDR RAM using a 135MHz bus.

The SmartMPEG-C device supports multiword DMA for ATA devices, and includes a USB 2.0 high speed OTG link controller for connection to USB hosts or devices.

Supporting the system is an advanced hardware acceleration unit capable of performing DMA operations including complex operations such as Triple DES encryption/decryption and RGB to 4:2:2 colour space conversion. The write-back unit behind the scaler, allows the implementation of a fast Mosaic mode.

The system is optimised for PVR applications with two video decoders and output units, three independent transport stream decoders and a hardware DMA controller.

The SmartMPEG-C comes with the Fujitsu Driver Application Programming Interface (FAPI) to help customers achieve the shortest possible development cycle. FAPI is a complete driver set allowing fast and efficient customer software design. In addition Fujitsu provides the PVR middleware, which offers stable handling for recording, playback, timeshift and trick modes.

### Features

- ARC Tangent-A4 CPU@202.5MHz (4k I-cache, 2k D-cache)
- Bootable from NOR or serial flash
- 16-bit 135MHz DDR RAM shared memory interface
- Unified memory system
- USB 2.0 high speed OTG controller
- Triple DES encryption and decryption
- Advanced hardware acceleration unit with DMA
- Multiword DMA ATA interface (16MByte/second)
- Universal processor interface (NAND/NOR Flash & common interface)
- Three transport stream decoders
- 3 DVB descramblers
- 2 hardware MPEG-2 video decoders MP@ML
- 2 flexible MPEG video resizing units (factor 1/16 to 2)
- 4-layer display controller (true-colour or CLUT) including YC<sub>R</sub>C<sub>B</sub> and RGB colour space
- Individual CLUT, Flicker and Flutter fixer for each layer
- Flexible frame rate conversion (50/60Hz)
- Teletext/WSS/PDC/CC/VBID insertion
- Cross Colour/Cross Luminance Filters
- PAL/NTSC/SECAM digital encoder
- RGB De-matrix (RGB or YP<sub>R</sub>P<sub>B</sub> output)
- ITU-R 656 video input & output
- Progressive output
- LCD output channel for connection to LCD panels
- 5 DACs for analogue video and audio output
- Hardware MPEG audio decoder (Layer 1/2)
- S/P-DIF output for PCM/AC3/MPEG, Dolby® Digital 5.1
- UART/2xSmart-card/I<sup>2</sup>C/GPIO/PWM Output
- 7-segment LED and 5 digit keypad controller
- General-purpose I/O controller
- Infra-red receiver/transmitter
- Internal clock recovery (no VCXO required)
- BGA256 or FBGA240 (10mm x 10mm) package/ambient temperature: 0 to 70°C
- Fujitsu CMOS 90nm technology 1.2V core, 3.3V I/O, 2.5V DDR
- Low power consumption: 450mW (Typ.)

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