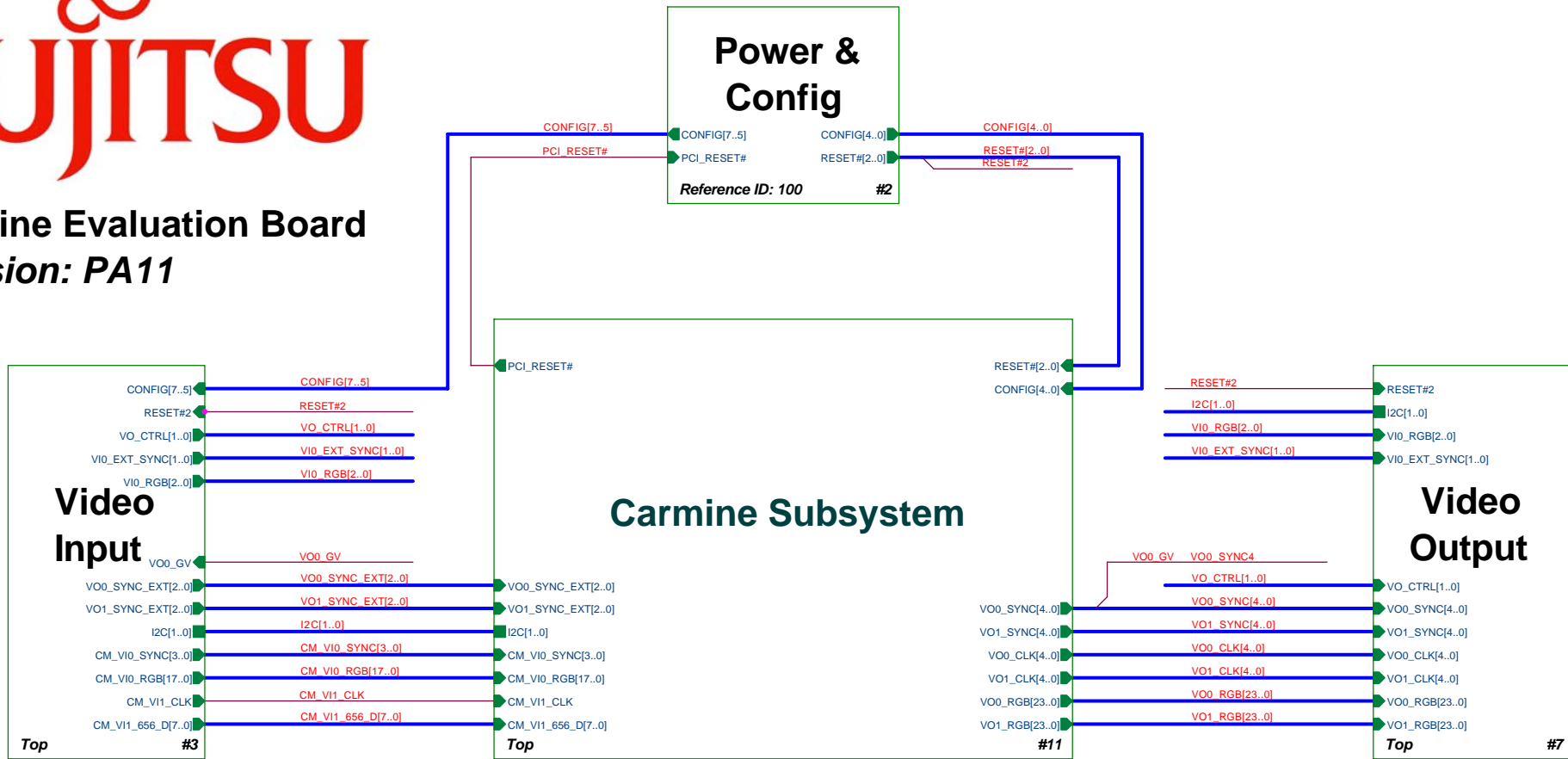




# Carmine Evaluation Board

## Revision: PA11



Hierarchy	Part References
+---#1 Carmine Eval Top	
+---#2 Power	1xx
+---#3 Video Input	
+---#4 RGB Input	2xx
+---#5 YUV Input	3xx
+---#6 Vi n Selector	4xx
+---#7 Video Output	
+---#8 RGB Output	5xx
+---#9 DVI Output	6xx
+---#10 LVDS Output	7xx
+---#11 Carmine Subsystem	
+---#12 Carmine	8xx
+---#13 Carmine Power	8xx
+---#14 PCI	8xx
+---#15 DRAM	9xx

I2C Address Map				
Device	Function	Write	Read	
U200 AD9883	RGB input ADC	0x98	0x99	
U300 SAA7113	composite video in #0	0x48	0x49	
U301 SAA7113	composite video in #1	0x4a	0x4b	
U400 XC2C128*	video input selector	0x60	0x61	
U600 SIL164	DVI transmitter #0	0x70	0x71	
U601 SIL164	DVI transmitter #1	0x72	0x73	

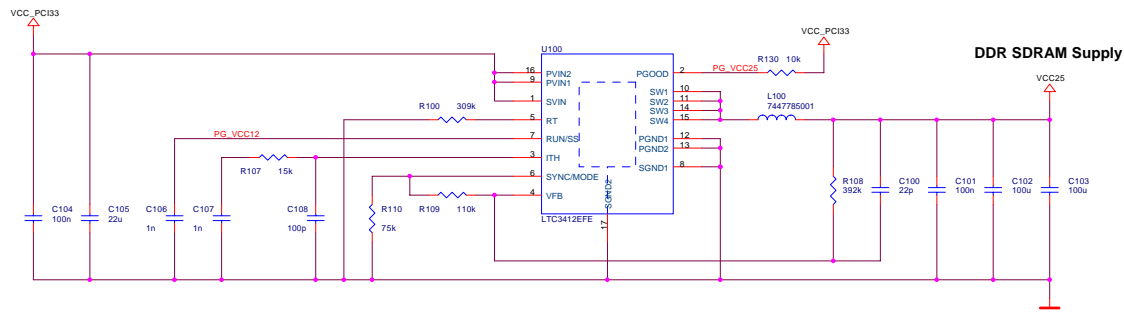
\* I2C address of video input selector depends on CPLD implementation

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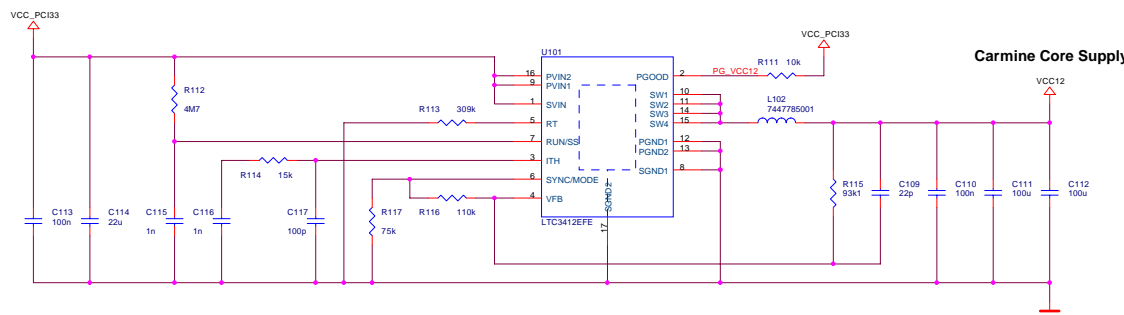
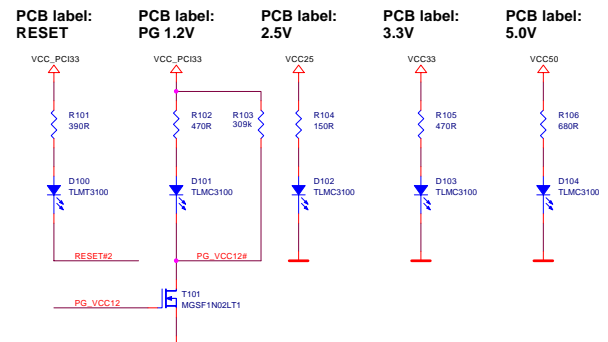
Title: Fujitsu Carmine Evaluation Board

Size: A3	Document Number: 30100-001	Rev: PA11
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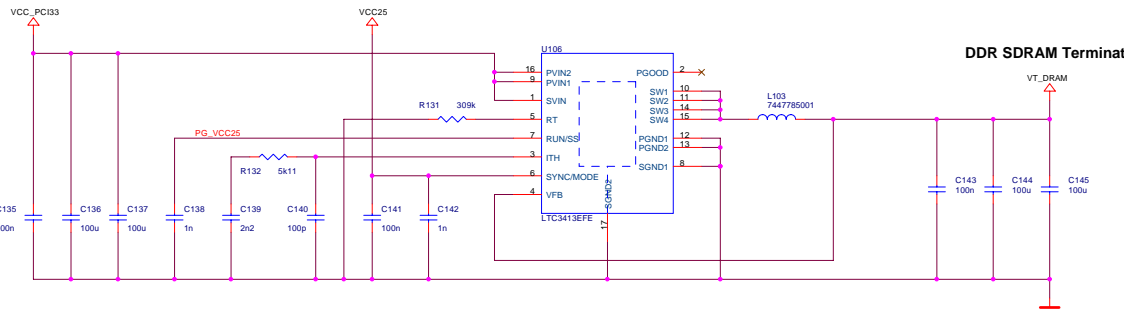
Date: Monday, November 21, 2005 Sheet 1 of 15



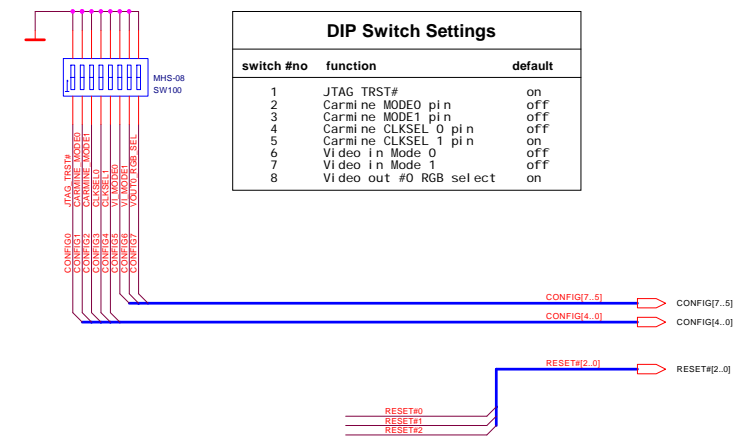
DDR SDRAM Supply



Carmine Core Supply

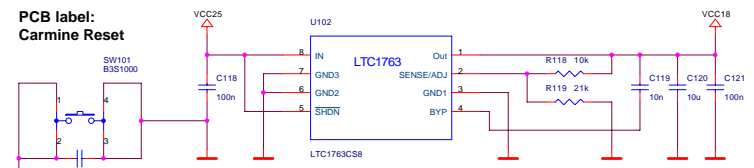


DDR SDRAM Termination

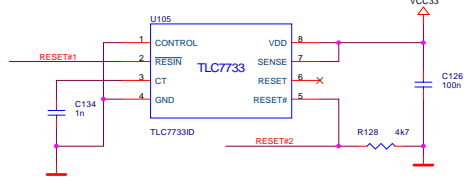


DIP Switch Settings

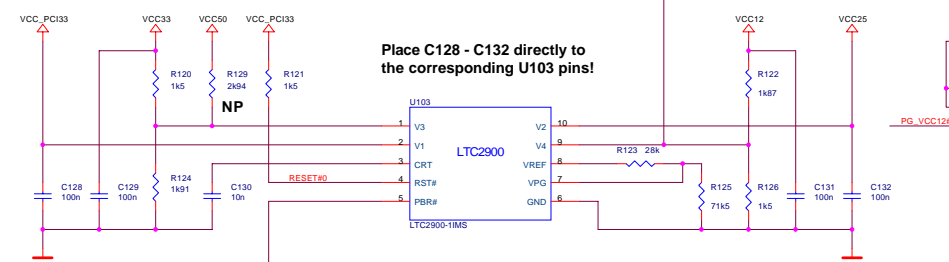
PCB label: Carmine Reset



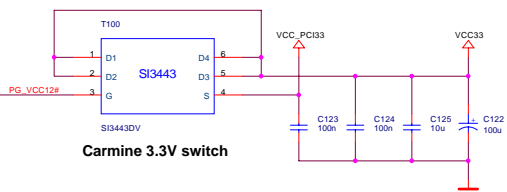
Video Input Selector CPLD Supply



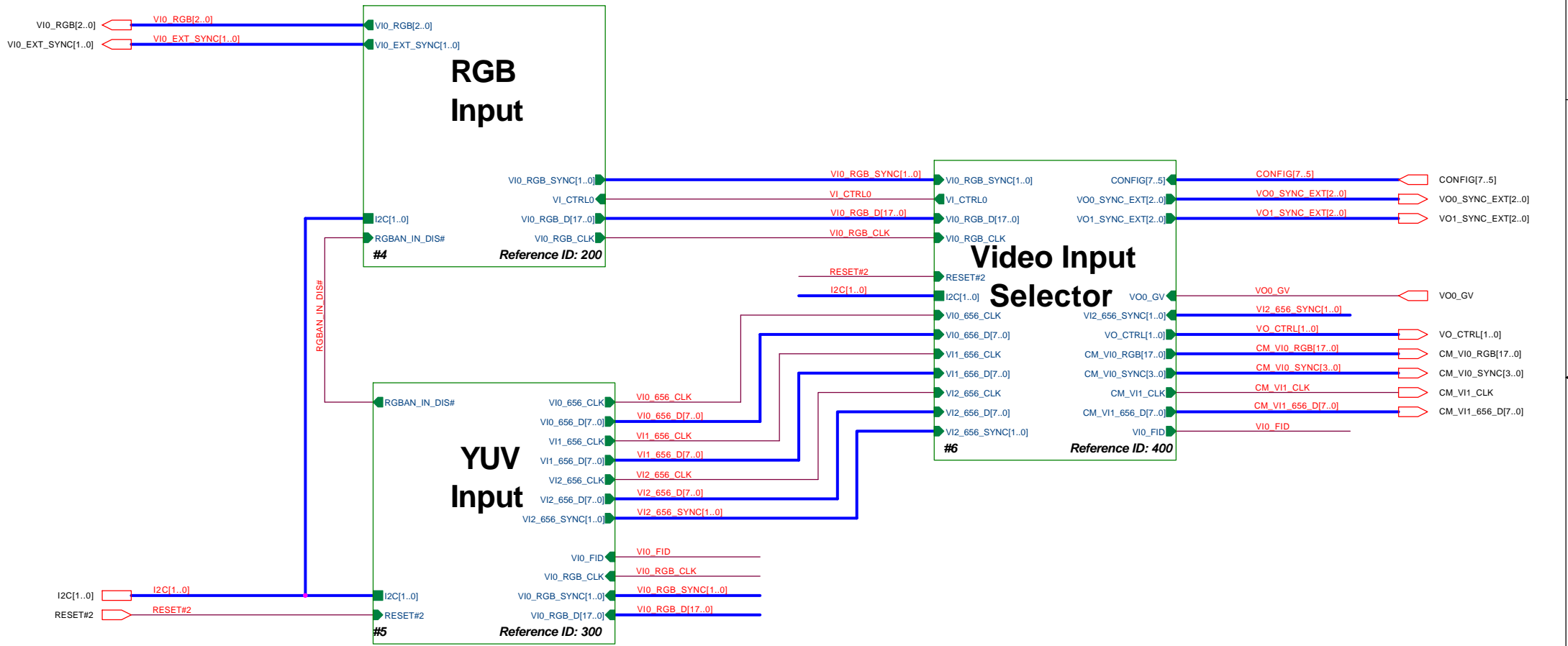
Place C128 - C132 directly to the corresponding U103 pins!

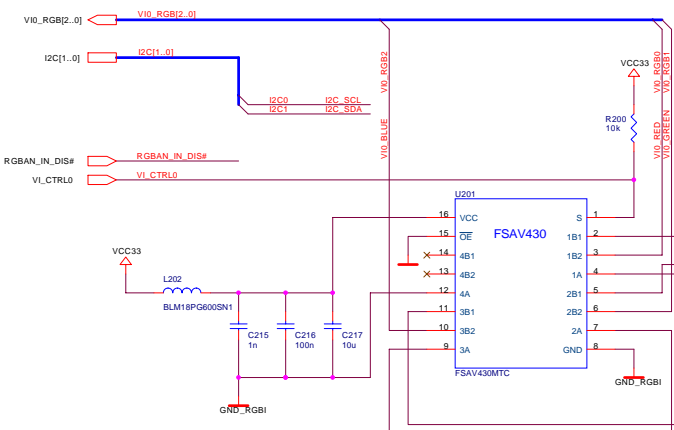


Carmine 3.3V switch



PCL\_RESET# → PCL\_RESET#

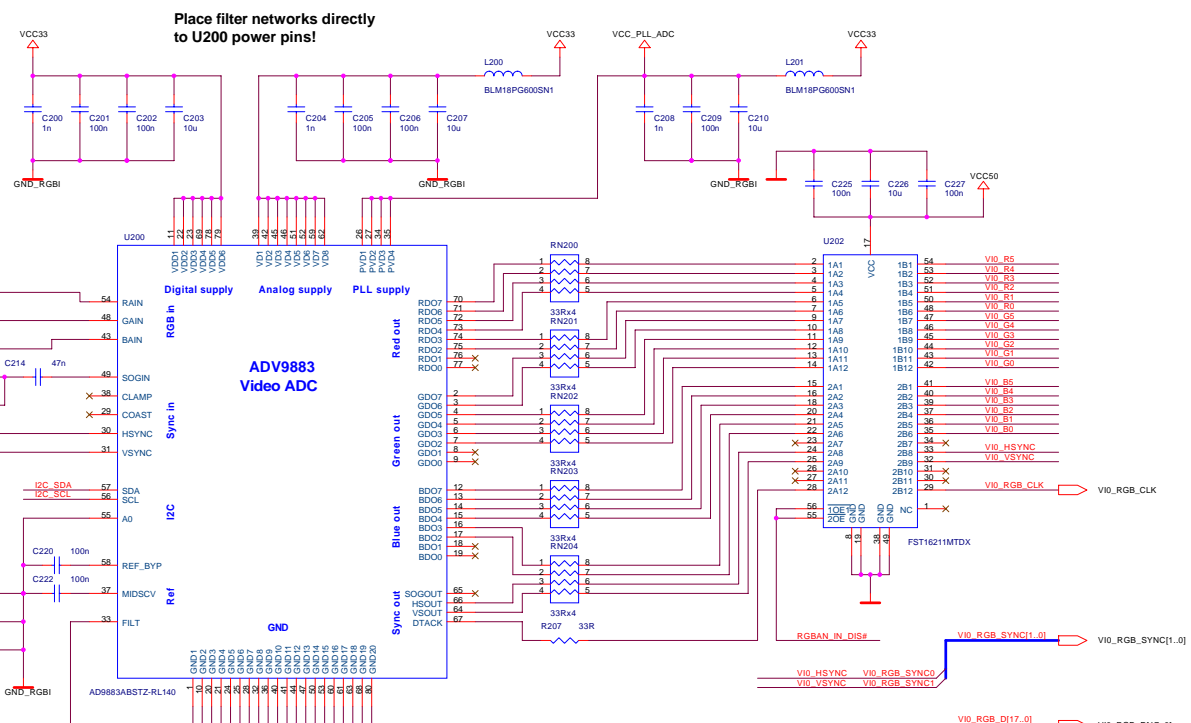




Place filter network directly to U201 power pins!

Short traces, no vias for all analog signals!

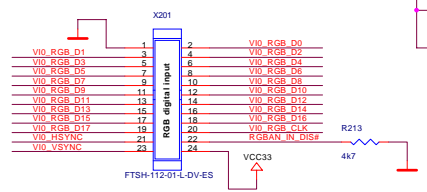
I2C addresses of ADV9883 read: 0x98, write: 0x98



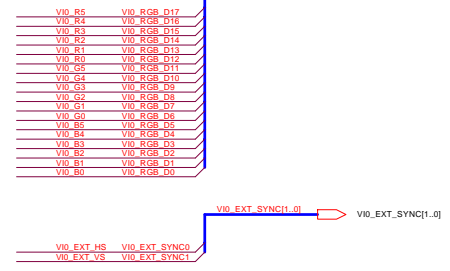
Place filter networks directly to U200 power pins!

Consider ADV9883 layout rules!

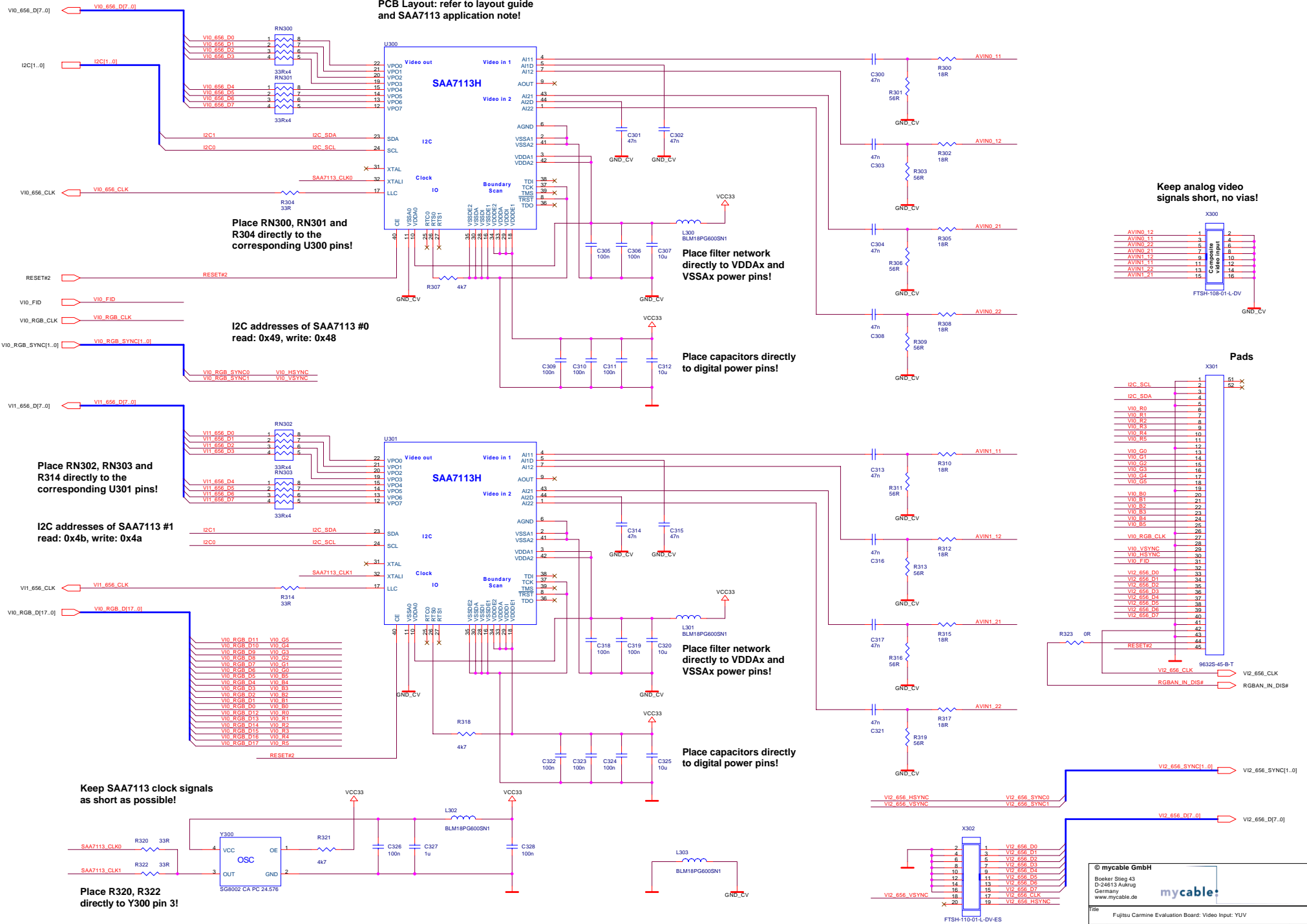
Place RN200 - RN204, R207 directly to the corresponding U200 pins!



Digital RGB input cable must tie pin 22 and 24 together in order to avoid digital RGB input bus conflict with ADC!



PCB Layout: refer to layout guide and SAA7113 application note!



Place RN300, RN301 and R304 directly to the corresponding U300 pins!

I2C addresses of SAA7113 #0 read: 0x49, write: 0x48

Place RN302, RN303 and R314 directly to the corresponding U301 pins!

I2C addresses of SAA7113 #1 read: 0x4b, write: 0x4a

Keep SAA7113 clock signals as short as possible!

Place R320, R322 directly to Y300 pin 3!

Place filter network directly to VDDAx and VSSAx power pins!

Place capacitors directly to digital power pins!

Place filter network directly to VDDAx and VSSAx power pins!

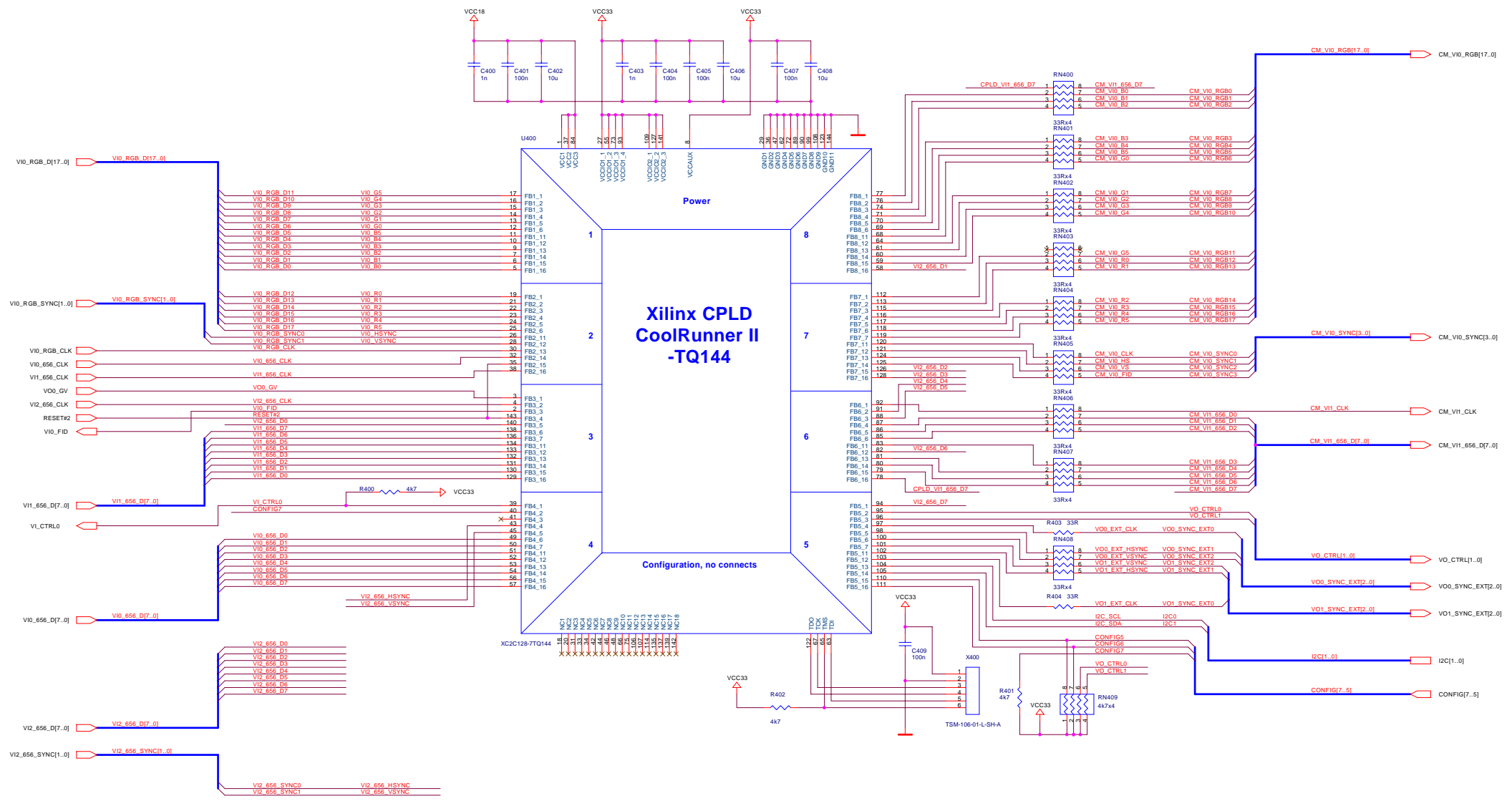
Place capacitors directly to digital power pins!

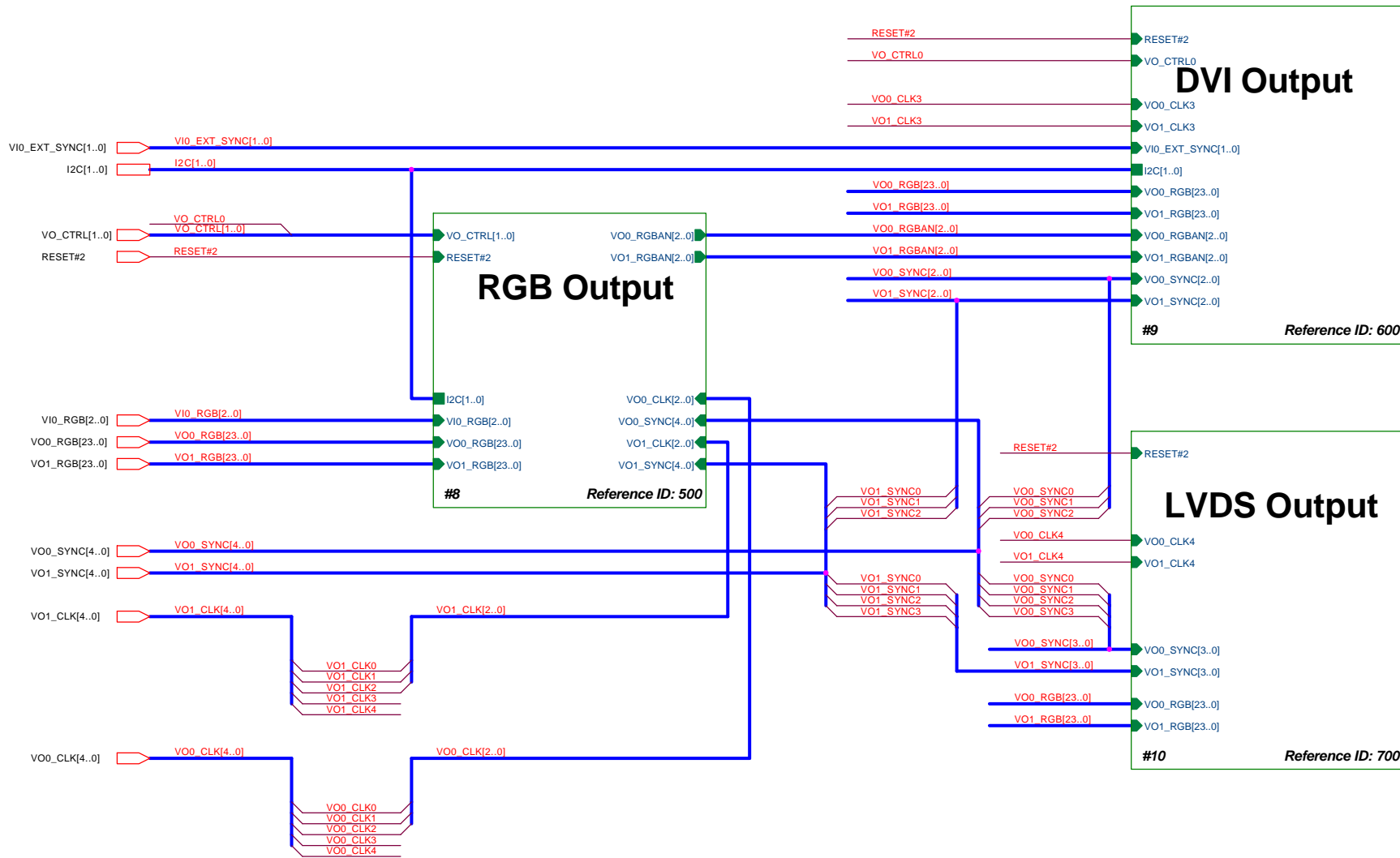
Keep analog video signals short, no vias!

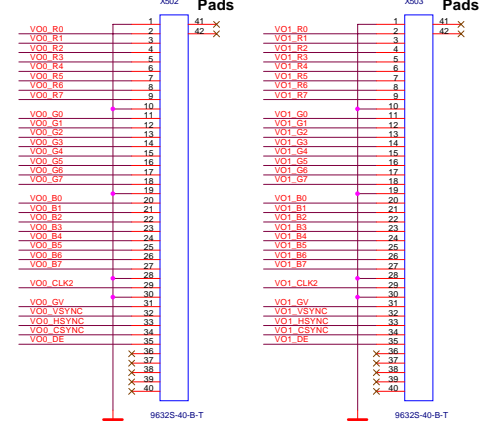
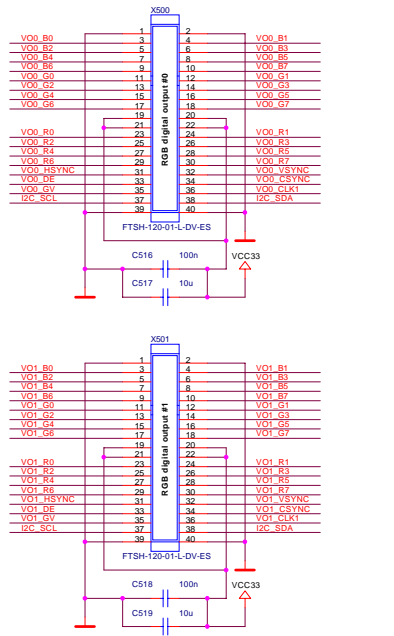
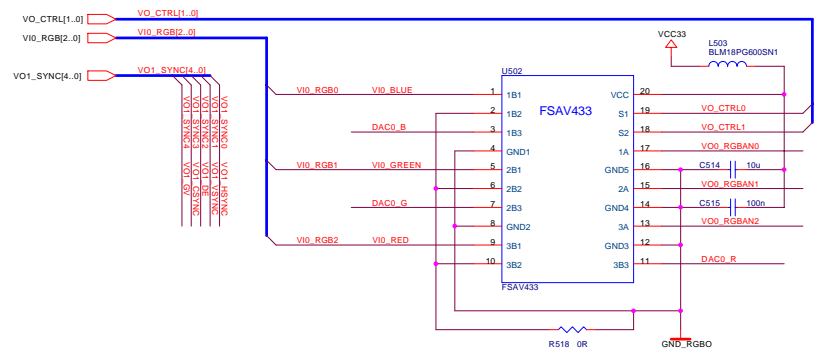
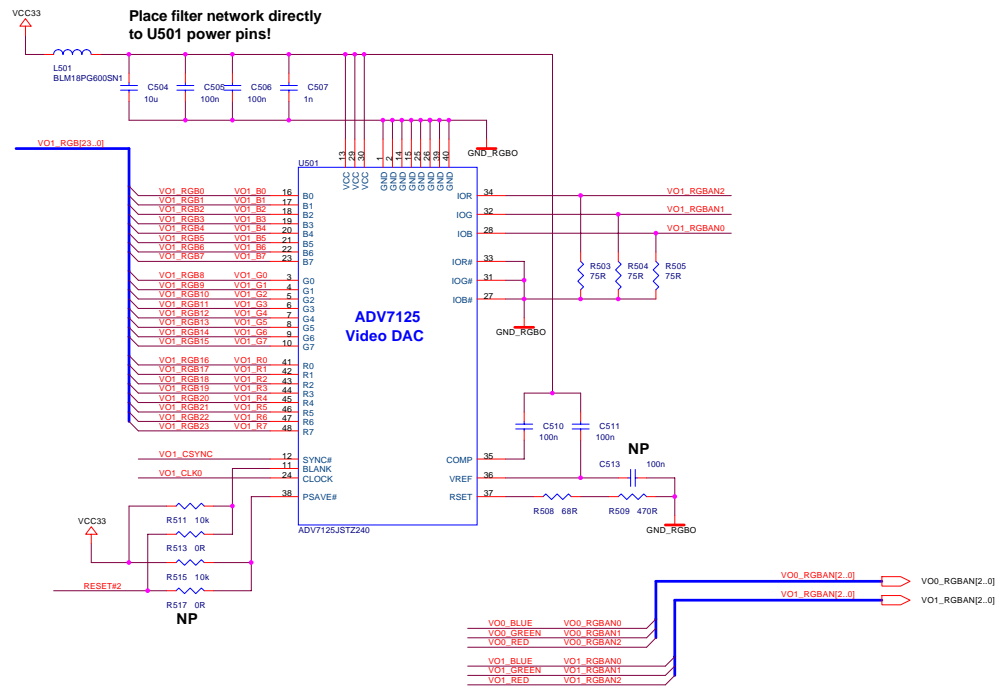
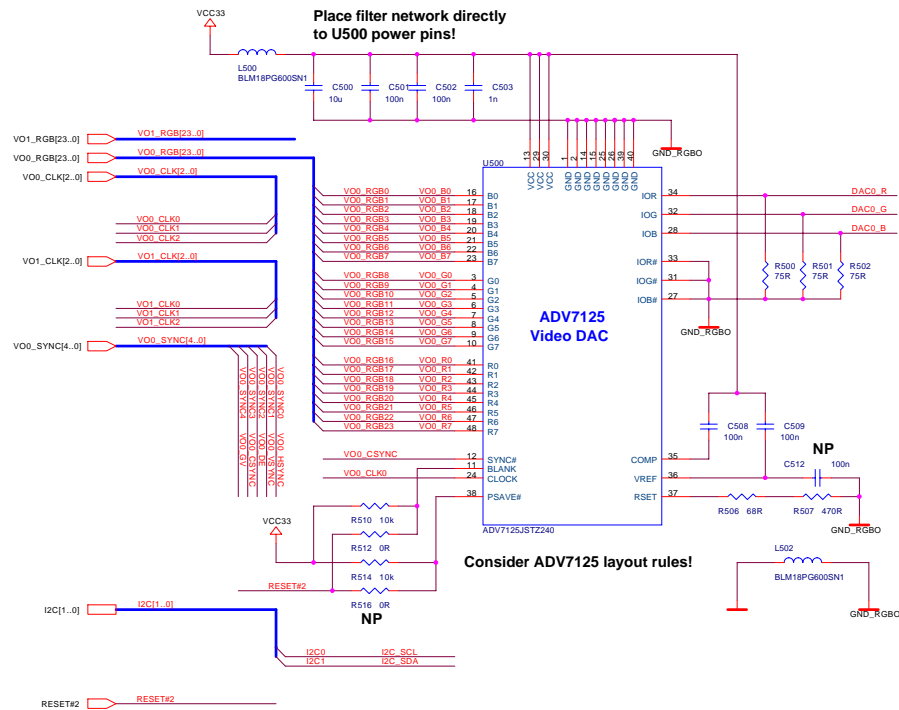
Pads

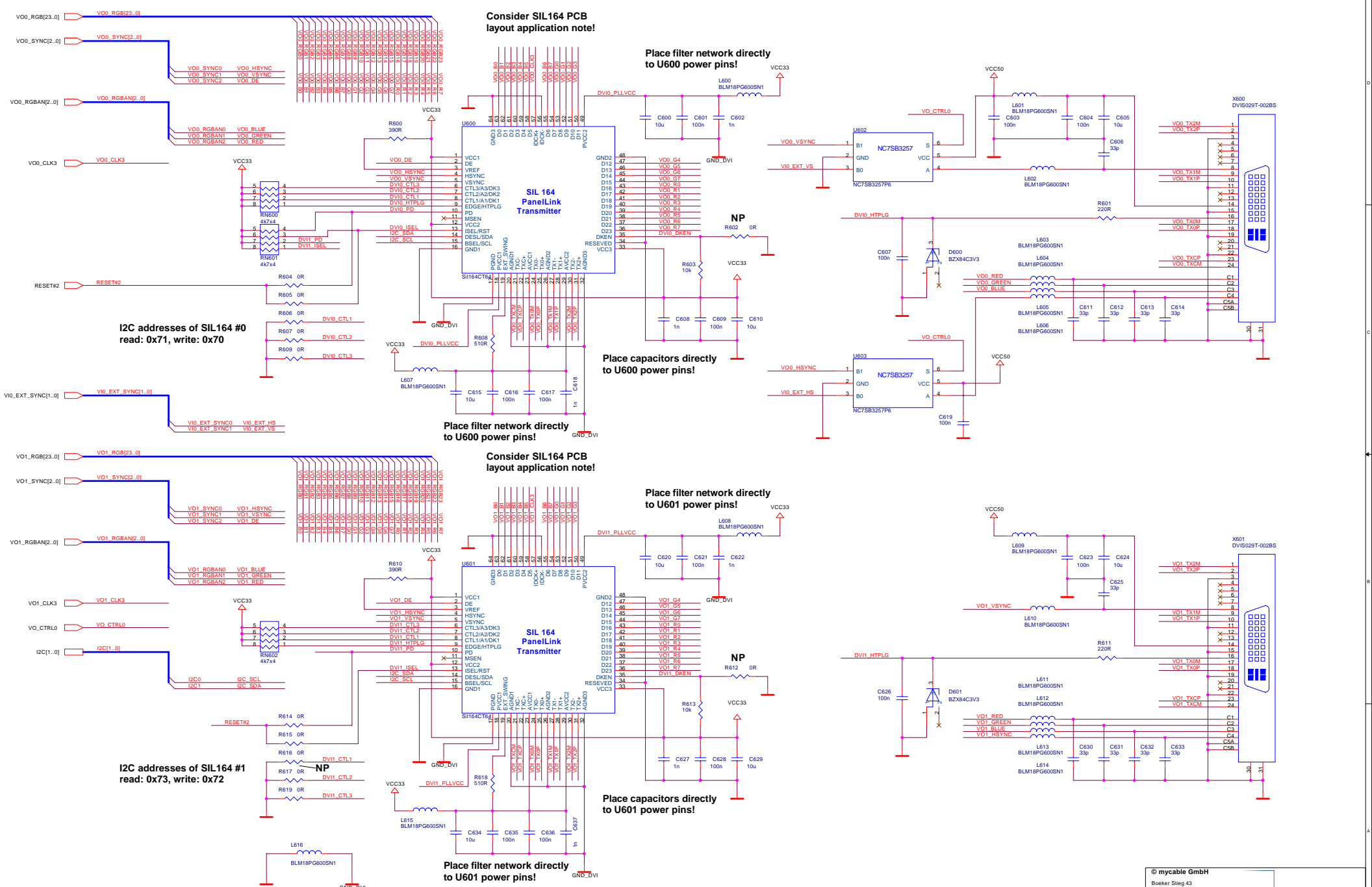
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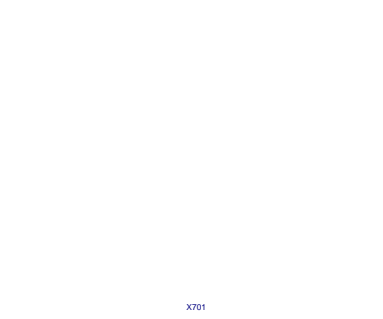
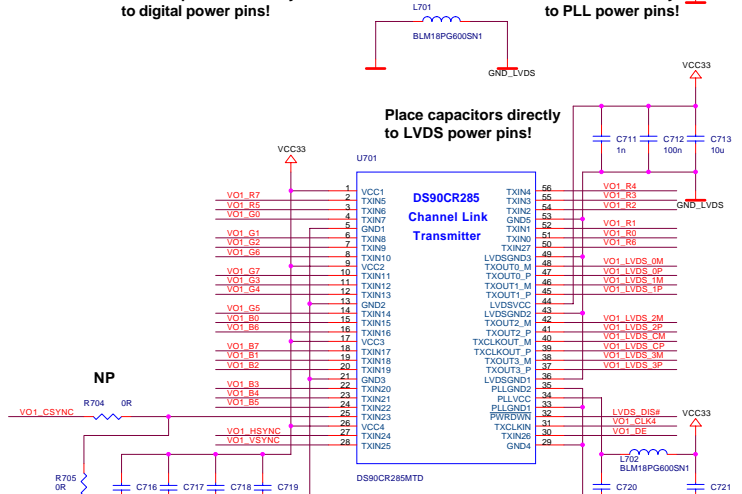
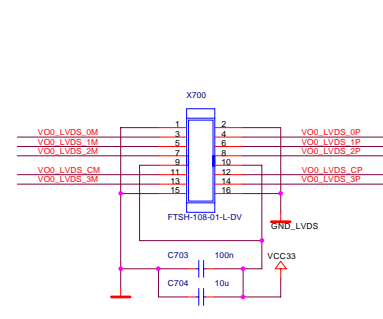
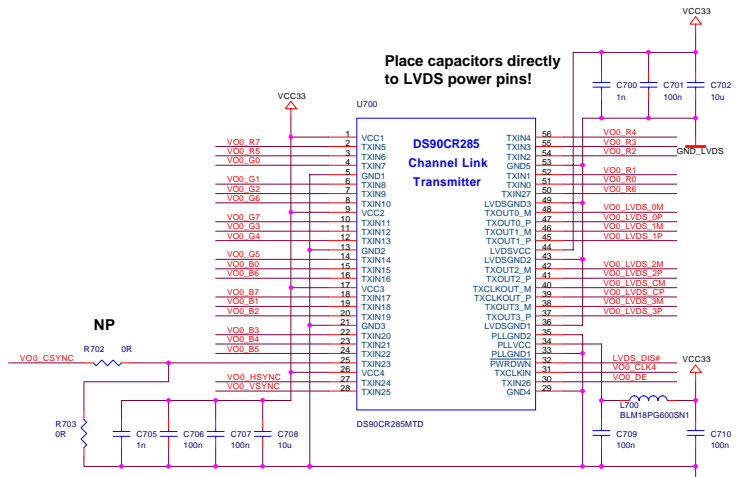
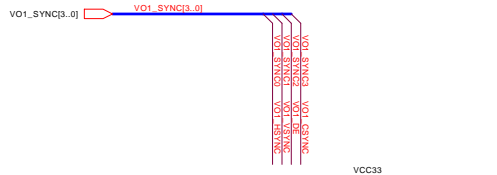
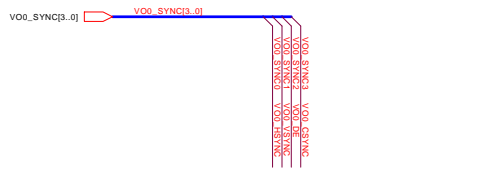
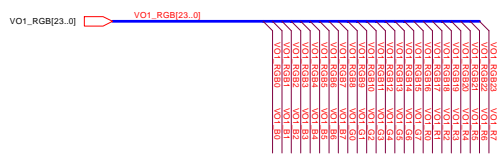
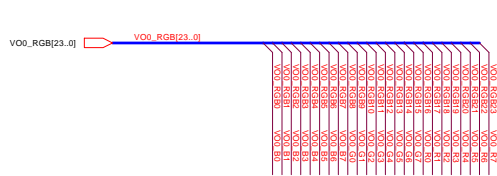
Place capacitors directly to U400 power pins!







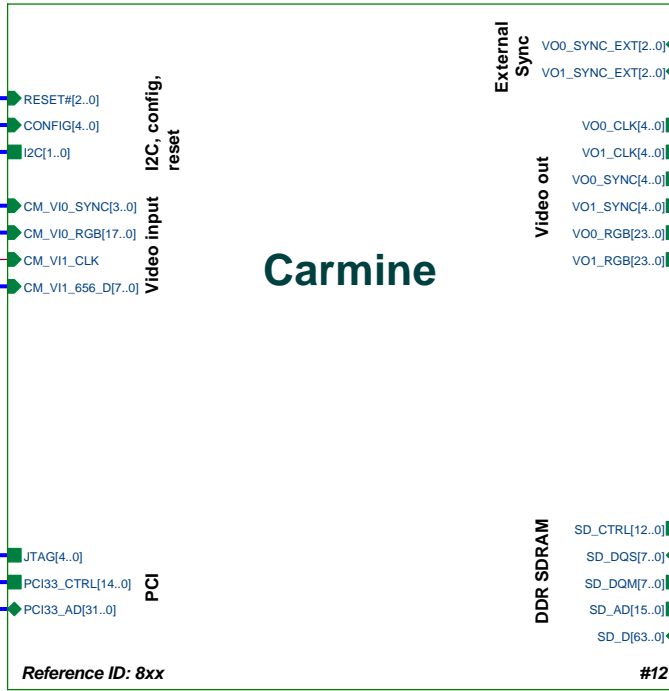




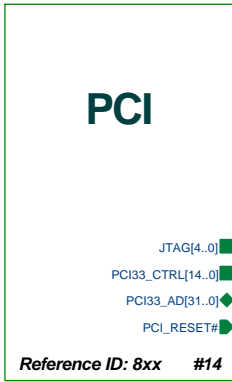
# Carmine Power

Reference ID: 8xx, 9xx #13

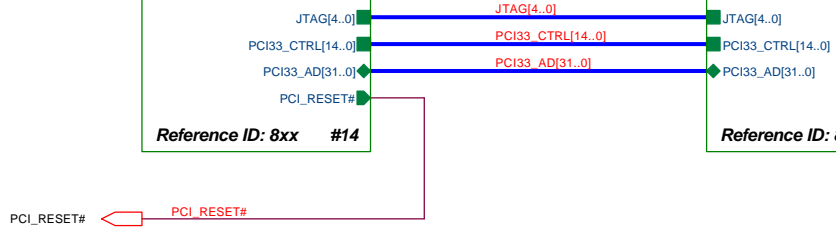
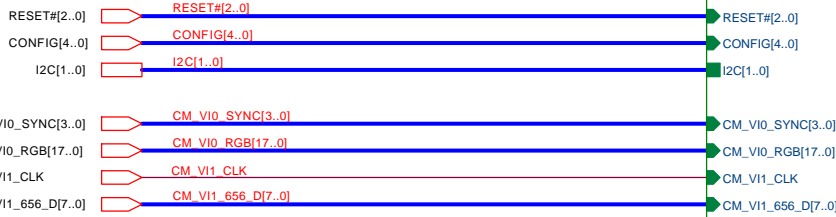
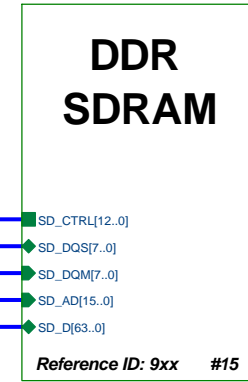
# Carmine

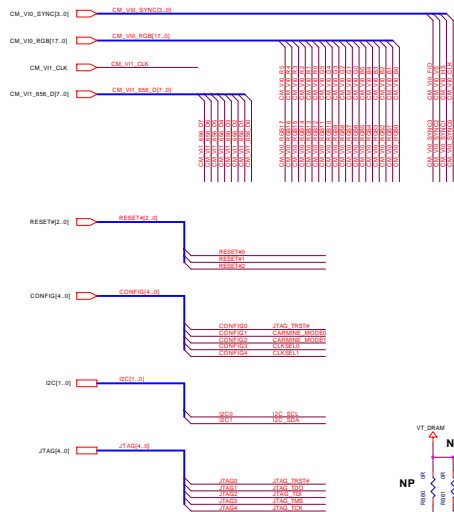


## PCI

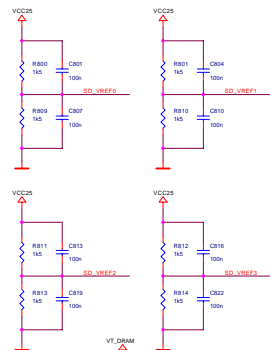


## DDR SDRAM

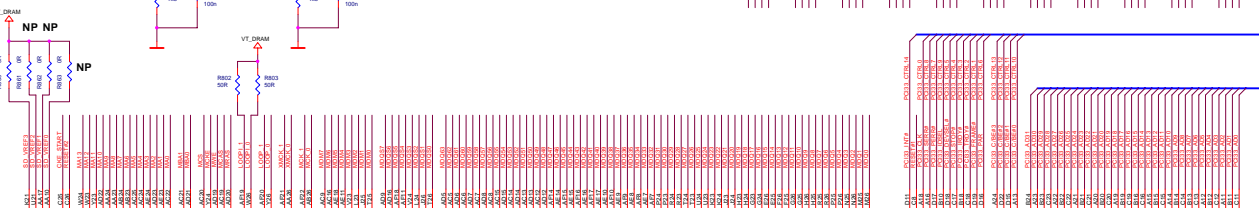




Place all DDR Vref networks directly to the corresponding Carmine pins!



Place all DDR damping resistors according to Carmine design guide!  
Consider DDR SDRAM layout rules from Carmine design guide!



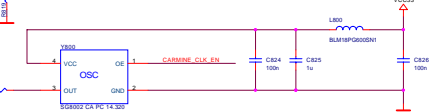
**Memory-Interface**  
**Carmine Graphics Processor**  
**PCI-Interface**

PCI Signal Assignment	
PCI_CTRL0	CLK
PCI_CTRL1	FRAME#
PCI_CTRL2	TRDY#
PCI_CTRL3	LDY#
PCI_CTRL4	STOP#
PCI_CTRL5	BEVSEL#
PCI_CTRL6	PAR
PCI_CTRL7	PERR#
PCI_CTRL8	SERR#
PCI_CTRL9	IDSEL
PCI_CTRL10	C/BE#
PCI_CTRL11	C/BE1#
PCI_CTRL12	C/BE2#
PCI_CTRL13	C/BE3#
PCI_CTRL14	INT#

Place R815 directly to U800 pin D7!

Place R820 directly to Y800 pin 3!

Keep Carmine clock signal as short as possible!



Place R829 - R833 close to the corresponding U801 pins!

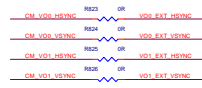
Clock skew adjustment NP

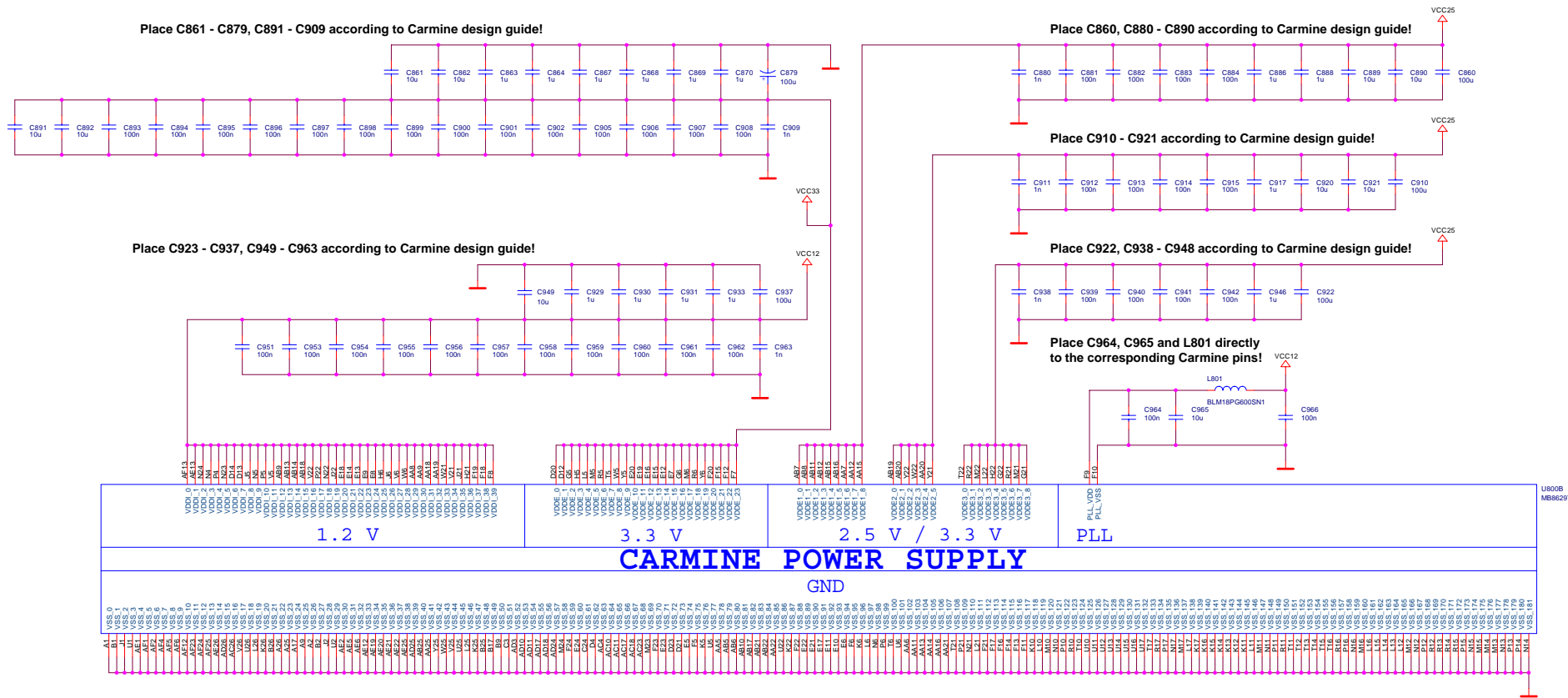
Place R834 - R837 close to the corresponding U802 pins!

Clock skew adjustment NP

Place R827, R828 directly to the corresponding Carmine pins!

Place R823 - R826 close to the corresponding Carmine pins!





Place C840 - C845 directly to the corresponding X800 power Pins!

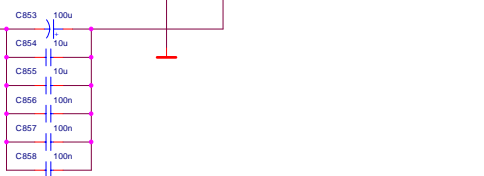


Place R847 directly to X800 Pin 16b!

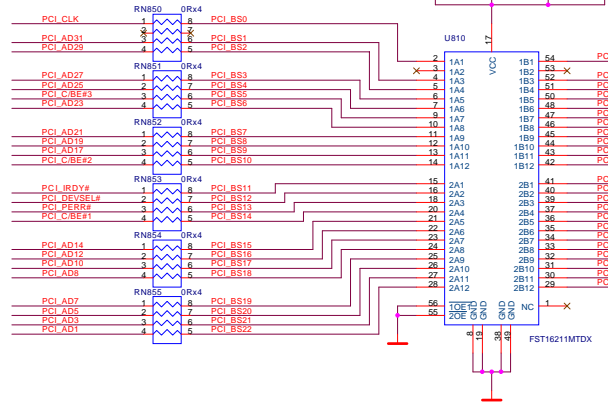
Place C852, R846 directly to PCI clock signal, no stub!

PCI clock routing according to PCB layout guidelines!

Place C853 - C858 directly to the corresponding X800 power Pins!

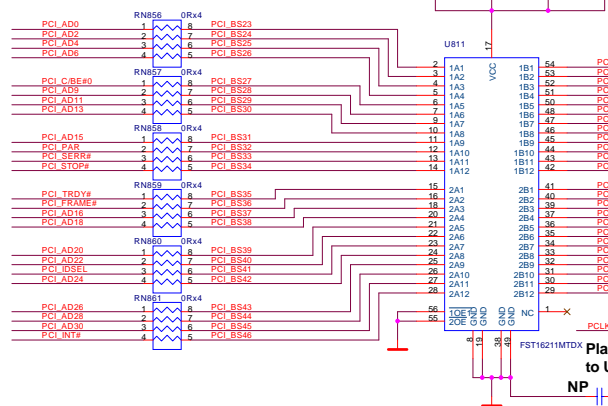


Place C846 - C848 directly to U810 power pins!



PCI Signal Assignment	
PCI_CTRL0	CLK
PCI_CTRL1	FRAME#
PCI_CTRL2	TRDY#
PCI_CTRL3	IRDY#
PCI_CTRL4	STOP#
PCI_CTRL5	DEVSEL#
PCI_CTRL6	PAR#
PCI_CTRL7	PARR#
PCI_CTRL8	SERR#
PCI_CTRL9	IDSEL
PCI_CTRL10	C/BE0#
PCI_CTRL11	C/BE1#
PCI_CTRL12	C/BE2#
PCI_CTRL13	C/BE3#
PCI_CTRL14	INT#

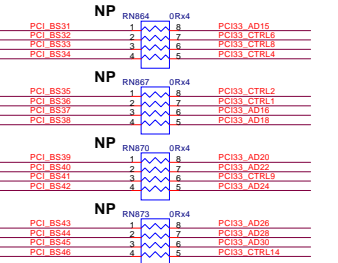
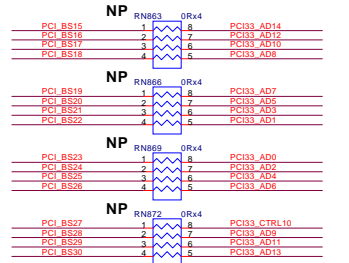
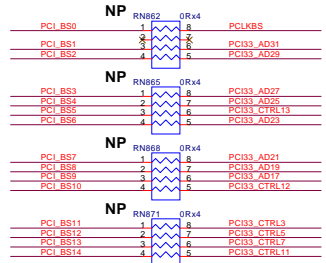
Place C849 - C851 directly to U811 power pins!



Place R848 directly to U811 Pin 29!

Place RN862 - RN873 under U810 and U811, on the same PCB side, no soldering paste on pads!

Place C859, R849 directly to PCI clock signal, no stub!



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