



FAQ list for Carmine

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History

Date	Author	Version	Comment
08.06.2006	AG	1.0	First release

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Graphic Controller frequently asked questions

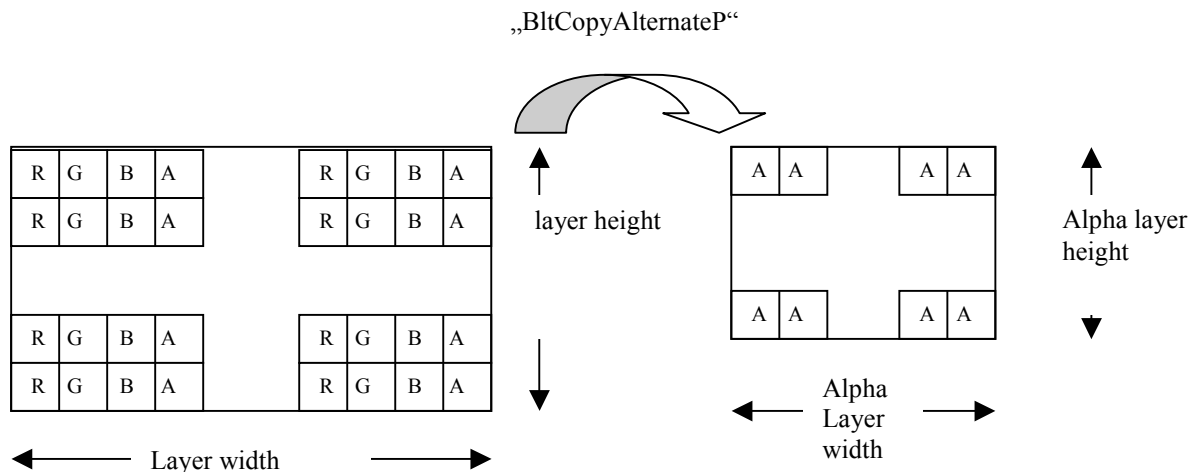
Jan 2006

Q1: RGBA layer blending directly

[back to top](#)

With layer 5, a RGBA layer can be blended directly, that means using the per pixel alpha value of that layer without using an alpha plane.

For all other layers pixel wise blending is only available with an alpha plane. The alpha plane can be extracted from an RGBA-layer with the BltCopyAlternateP command as shown below.



If an layer is drawn in RGBA-format the per pixel alpha value can not be used for alpha blending directly. To make the per pixel alpha value available for blending function, it needs to be extracted from the color data and be copied to an alpha plane.

The BltCopyAlternatP function of the Carmine supports that operation. BltCopyAlternateP copies data between different areas of the graphic memory.

Stride of source and destination layer need to be adopted to the format of these layers.

Because the width and height of that operation is limited to 4096x4096 pixel it may more than 1 BltCopy operation be necessary.

Q2: 2 video inputs at 1 output

[back to top](#)

It is possible, to display 2 video inputs on one video output.

One video layer can be used with full feature set.

One video layer must be set to:

-> RGB mode

-> no up scaling

-> single buffer mode

Q3: Is pixel clock output if display controller is disabled

[back to top](#)

Like on Coral, the pixel clock is output, even though the display controller is disabled via DCM register.

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Q4: blending with background color

[back to top](#)

yes, a layer can be blended with background color. Bit 31 of DBGCR register must be set to 1.

Q5: power consumption

[back to top](#)

Condition:

- Ta=27 degree Celsius
- hardware: evaluation board MB86297EB01
- VDDI=1.3V
- VDDE1,2,3 = 2.7V
- Cap0: 656 input
- Cap1: 656 input
- Display0: SVGA 8 layer
- Display1: SVGA 8 layer
- Kottos : Geometry, alpha, texture, depth test

It was measured current to 1.2V and 2.5V power net.

Note: Current consumption on 2.5V power is including DDR-SDRAMx4 and other small parts.
The other power current (3.3V, VTT) is calculated by simulation

Result:

- VDDI=0.81A
- VDDE1,2,3 = 0.9A

Board power consumption is :

$$0.81 \times 1.3 + 0.9 \times 2.7 = 3.483W \dots\dots(1)$$

1.3V power is used by only carmine

2.7V power is used by Carmine, DDR-SDRAM and other small parts
DDR SDRAM power consumption is calculated as follows <operating condition>

According to the catalog of K4H561638F(DDR266@CL2),
-IDD4R=170mA , IDD4W=165mA

We expect the read and write transaction occur alternately.

IDD4R

$$170mA \times 4 \times 2.7V = 1.836W$$

IDD4W

$$165mA \times 4 \times 2.7V = 1.782W$$

Power consumption is

$$(1.836 + 1.782) / 2 = 1.809W \dots\dots\dots(2)$$

VDDE, VTT power consumption based on simulation are as follow

$$VTT = 409mW \dots\dots(3)$$

(Just only consume carmine's DDR I/O. except for stub resistor and terminal resistor)

$$VDDE = 150mW \dots\dots(4)$$

Carmine power consumption is calculated as follow.

$$P = (1) - (2) + (3) + (4)$$

$$= 3.483 - 1.809 + 0.409 + 0.150 = 2.233W$$

Q6: terminating unused video input pins

[back to top](#)

The unused input pins need a high-impedance pull-down resistor.

Q7: JTAG interface / boundary scan

[back to top](#)

JTAG standard: IEEE std 1149. 1b-1994

BSDL file is available : MB8AA0130GYH_FME.bsd. The BSDL-file can be required from FME via email to mailto:gdc_info@fme.fujitsu.com

Indispensable Instruction(EXTEST,SAMPLE/PRELOAD,BYPASS) defined in IEEE1149.1 is supported by JTAG module.

Moreover, Instruction registers are 5 bits.

Don't leave JTAG pins open.

Unused JTAG pins are to terminate with pull-down-resistors.

Termination can be done directly without using pull-up-/ pull-down resistors.

Technology of JTAG pins : CMOS, more information on page 512 of hardware manual rev. 0.72

The JTAG support module does not support the I2C- interface and the memory interface for boundary scan. For more information about how to connect the JTAG module please refer to according application note.

Q8: are the mode pins 3.3V or 2.5V pins

[back to top](#)

The pins MODE[1:0] are 3.3V I/O.

Q9: suitable memory devices

[back to top](#)

Samsung K4H561638F

Micron: MT46V16M16TG

Q10: jitter value at the DOTCLK-signal

[back to top](#)

The jitter of the PLL output is 47 ps.

The frequency at the DOTCLK is calculated : PLL output frequency divided by N.

The jitter at the DOTCLK is calculated : (jitter of PLL output) x (square root of N)

e.g. $f_{\text{PLL}} = 533 \text{ MHz}$

$N = 20$

$f_{\text{DOTCLK}} = 26.65 \text{ MHz}$

jitter at the DOTCLK = $47 \text{ ps} * 4.472$