FAQ list for Coral

History

Date	Author	Version	Comment
08.10.2003	AG	1.0	First release
16.08.2004	AG	1.1	Q23 for Coral PA added
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Graphic Controller frequently asked questions

Jan 2003

MB86293,4,5 CORAL QUESTIONS :

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How are the different color-depths from the active layers processed internally for layer- and plane-alphablending ?

All pixels from the different color spaces (8bit/pixel palette, 16bit/pixel, 24bit/pixel and 16bit YUV) will be converted to RGB888 before any further operation. During this conversion, the lower 2 bits of the 8bit palette values (from RGB666 values) will always be set to 00. The 3 lower bits of 16bit/pixel (RGB555) values will be set to 000 if the color value is also zero, otherwise to 111. The YUV values from the video input will be converted to RGB888 using a YUV->RGB conversion matrix. Then the available RGB888 values will be displayed (priority order) or blended together with the other layer values. At the output stage, an RGB888 value is available which can be used to drive a display directly or which can be converted to analog using a DAC.

Q2: back to top
How are the alpha-blending values calculated ?

If alpha-blending is enabled for a particular layer, all pixel colors are calculated according to the formula :
C = C1 * A + (1-A) * C2
where :
C is the resulting pixel color
C1 is the 1st layer color
C2 is the 2nd layer color
A is the blending coefficient A=alphavalue/255

thus :
Alpha=0 -> A=0 -> C = C2
Alpha=255 -> A=1 -> C = C1
Alpha=128 -> A=0.5 -> C=0.5*C1 + 0.5*C2

Note that there are 2 possibilities :
1.) All Alpha-values for one layer are constant (layer blending mode)
2.) Each pixel can have a different alpha-value (alpha map mode)

Q3: back to top
How many layers can be used simultaneously with Coral ?

Coral bandwidth estimation :

Conditions:
Display: Resolution=800x480, Dot clock=33.3MHz,
All layers(windows) are 800x480 size.
Graphic Memory: Clock=133MHz, Memory data width=64bit,Memory model=SDRAM
Bus Traffic: No video capture, constant drawing operations

Simulation results :

1. 16BPP:0 layers and 8BPP:6 layers => OK
2. 16BPP:1 layers and 8BPP:5 layers => OK
3. 16BPP:2 layers and 8BPP:4 layers => OK
4. 16BPP:3 layers and 8BPP:3 layers => OK
5. 16BPP:4 layers and 8BPP:2 layers => NG
6. 16BPP:5 layers and 8BPP:1 layers => NG
7. 16BPP:6 layers and 8BPP:0 layers => NG

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What is the level of the clock input pin (CLKIN) of Coral ?

The CLKIN Pin has a 3V3 level.
On the evaluation board, the CLKIN pin is connected with the 74LVC04APW.
This chip is a 3V device, but it is also possible to use a 5V swing.

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How about Coral B's power consumption ?

typical values:

3.3V: 100mA
1.8V: 500mA
estimated power consumption: 1.23W

Q6: back to top
How about Coral P's power consumption ?

typical values:

3.3V: 90mA
1.8V: 500mA
estimated power consumption: 1.251W

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What memory can be connected to Coral? How is it to connect to Coral?

The memory controller of Coral supports simple connection with SD/FCRAM by setting MMR(Memory Mode Register). If there is N(=11 to 13) address pins in SD/FCRAM, please connect the SD/FCRAM address(A[n]) pin to the Coral's memory address(MA[n]) pin and SD/FCRAM bank pin to the Coral's next address(MA[N]) pin. Then please set MMR by a number and type of memory.

The follows are the connection table between Coral pin and SD/FCRAM pin.

64M bit SDRAM (x16 bit)		**64M bit SDRAM (x32 bit)**	
Coral	**SDRAM**	**Coral**	**SDRAM**
MA[11:0] MA12 MA13	A[11:0] BA0 BA1	MA[10:0] MA11 MA12	A[10:0] BA0 BA1

128M bit SDRAM (x16 bit)		**128M bit SDRAM (x32 bit)**	
Coral	**SDRAM**	**Coral**	**SDRAM**
MA[11:0] MA12 MA13	A[11:0] BA0 BA1	MA[11:0] MA12 MA13	A[11:0] BA0 BA1

128M bit SDRAM (x16 bit)		**128M bit SDRAM (x32 bit)**	
SDRAM	**Coral**	**SDRAM**	**Coral**
MA[12:0] MA13 MA14	A[12:0] BA0 BA1	MA[10:0] MA11	A[10:0] BA

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What is the pin assignment for the RGB888 (multiplexed) video input of Coral P ? In the manual only the direct RGB666 video input is explained.

The pin assignment is shown in the following table :

Direct	Multiplex
GI [5] GI [4] GI [3] GI [2] GI [1] GI [0]	GI [7] GI [6] GI [5] GI [4] GI [3] GI [2]
|BI [5] |BI [4] |BI [3] |BI [2] |BI [1] |BI [0]	RB [7] RB [6] RB [5] RB [4] RB [3] RB [2]
|RI [5] |RI [4] |RI [3] |RI [2] |RI [1] |RI [0]	RB [1] RB [0] GI [1] GI [0] COLSEL

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Coral P PCI bus test

1.) How can the pins of the PCI bus be put in tri-state mode ?
The following conditions are required in order to set each pin to Hi level, Low level, and Hiz.

AD0..31, CBE0..3, PAR, FRM, IRDY
Hi level : When Coral operates as PCI master read/write burst.
Low level : When Coral operates as PCI master read/write burst.
Hiz : Under reset or after reset.

TRDY, STOP, DSEL
Hi level When Coral operates as PCI slave read/write.
Low level When Coral operates as PCI slave read/write.
Hiz Under reset or after reset.

REQ
Hi level After reset.
Low level When Coral operates as PCI master read/write burst.
Hiz Under reset.

PERR
Hi level When Coral operates as PCI slave read/write.
Low level When Coral operates as PCI slave read/write and parity error occurs in data phase.
Hiz Under reset or after reset.

SERR (open drain)
Low level When Coral operates as PCI slave read/write and parity error occurs in address phase.
Hiz Under reset or after reset.

XINT
Low level When interrupt occurs.
Hiz Under reset or after reset.

2.) What is the effect of a reset (XRST, Firm RESET) with respect to these pin levels ?
It is set to following level after reset.

AD0..31 Hiz
CBE0..3 Hiz
PAR Hiz
FRM Hiz
TRDY Hiz
IRD Hiz
STOP Hiz
DSEL Hiz
PERR Hiz
REQ Hi level
SERR Hiz
XINT Hiz

3.) What happens if Coral does not get a bus grant after a REQ demand issued by Coral ?
If Coral does not get a bus grant after a REQ demand issued by Coral,
It continues waiting for bus grant.
In the meantime, it is possible to access to Coral as PCI slave.

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The manual of Coral P says, that texturing in 24 bit/pixel mode works. Is Coral P really able to render a 24bit/pixel texture into a 24bit/pixel layer ? Or is Coral P only able to render a 24 bit/pixel texture into a 16 bit/pixel layer ?

All Coral devices do NOT support texture mapping in 24 bit/pixel.
The page 91 of section 10.4.2 Texture color is wrong. We will revise it.
Coral-Q/B/P support just 8/16 bit/pixel texture mapping.

The reason of this mistake is that Coral-ES (first eva-chip of Coral)
supported the 24 bit/pixel rendering and texture mapping.
But this function was taken out since Coral-Q.

Q11: back to top
Possibility of simultaneous up/down-scaling with Coral P (MB86295).

In principal, up-/down scaling does work, if an odd value is set to CIHSTR.
But the beginning few pixels (9 pixels) are not captured. So CIHSTR value plus 9 pixels are not captured.

Note : Coral P was not designed for simultaneous up/down scaling.
The Cb data and Cr data are exchanged when up/down scaling is selected.
The reason of the Cb and Cr swap is a different latency between up- and down-scaling.
But if the CIHSTR register is set to an odd value, it will overcome this problem with the restrictions mentioned above.
In Coral PA, this will be corrected.

The missing pixels are the case for the beginning first few pixels of each line at each frame.
Therefore it seems like the frame is shifted to the left.
This phenomenon occurs only at the combination of up and down
scaling. (Example, horizontal up scaling and vertical down scaling)

These settings are usable under the same conditions of the others settings.
(TA: -40 to +85 deg C, VDDL:1.65 to 1.95V, VDDH:3.0 to 3.3V)
Not all the pixels are captured as explained, but the capturing and displaying process works stable.

The WEAVE mode can not be used in vertical up-scaling mode.
So if vertical down-scaling and horizontal up-scaling is selected, the WEAVE mode can be used.
But there is the same restriction as in the BOB mode (the first few pixels are not captured).

Q12: back to top
Coral-Q temperature

- thermal resistance junction - package
16 degC/W

- max. junction temperature
117 degC

- max. power dissipation
typical (measurement eva-board, Host I/F: 33MHz, GE: 166MHz, OT: 133MHz)
1.8V : 480mA
3.3V : 50mA

max (Host I/F up to 100MHz)
1.8V : 960mA
3.3V : 200mA

Q13: back to top
Coral timing. Why doesn't the timing correspond to the indicated values the timing registers?

The start point for HSP has a latency of 14 clocks.

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What is the time relation (delay) between DCLKI and DCLKO in the external display clock mode ?

This delay time is not controlled as spec , it is different with each product series. We show them as reference values.
For Coral-LP, max=11.1ns and min=5.4ns.

Q15: back to top
unused YUV inputs

In case of NOT using video capture, you just have to set these signals to "High" or "Low".

But in case of Coral-LB and LP, the video capture signals are multiplexed with graphics memory bus.
Therefore please connect to "high" or "low" level by pull-up/down resistor.

In case of Scarlet, the video capture signals are not multiplexed with memory bus.
Therefore please connect to "GND" or "VDD" directly.

additional info:

what are the consequences if unused video input pins are left open ?

There is no special notices for Coral-P.
It is the same for all of CMOS devices.

Leaving pins open can destroy the pad cells by static electricity or latch-up and finally the destroyed the device,because of the direct tunneling current.

Q16: back to top
Performance Test - Coral-P

- resolution : 800x480
- Geometry clock frequency : 166MHz */
- Other clock frequency : 133MHz */
- pixel clock : 33,4MHz - 0x0b00

- (Capture-layer - L1) + (16bpp-layer - L0, L2, L3)x3 + (8bpp-layer - L5, Alpha-plane)x1

The following conditions are possible to use in the 32-bit bus width with "Drawing".

- (Capture-layer) + (16bpp-layer)x2 + (8bpp-layer)x1
- (Capture-layer) + (16bpp-layer)x3

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New function of CBM register at Coral-P:

CBM register (Address: Capture Base+0x010)

Bit-0, CBST(Capture Burst) bit

Select the burst length for writing the captured data to graphics memory. This function is used when the saturation is occurred.

CBST=0 Default (4 words burst)
CBST=1 Long Burst (8 words burst)

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Coral DCLKO Duty-Cycle

A duty of DCLKO signal made by a internal PLL output is depended on setting of SC bit in DCM/DCEM register.

If you set scale value to SC bit of DCM register, a duty of DCLKO signal are always 50%.

If you set scale value to SC bit of DCEM register, it is depended on scale value.
If frequency division rate is even number, a duty is 50%.
If it is odd number, pulse ratio of L:H is (n+1):n.

(Example)
1)SC bit of DCEM = 12 (Frequency division rate = 1/13)
L:H of DCLKO => 7:6
1)SC bit of DCEM = 36 (Frequency division rate = 1/37)
L:H of DCLKO => 19:18

Note)
The follows values are not considered PLL jitter.
Regarding PLL jitter, please refer hardware manual.
And if you need exact 50% duty dot clock, please input clock from DCLKI pin.

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a question for the Coral P internal PLL.

I need to use an internal PLL frequency of 398MHz to get the correct display timings.
According to the Coral specification, it is possible to use a 14.22MHz oscillator (allowed range for CLKSEL=01 is 14.177...14.32MHz).
The question is :
Will the PLL generate 14.22MHz * 28 = 398.16MHz internally - or will the PLL output 400.909MHz anyway in this mode ?

The PLL generates 398.16MHz when 14.22MHz.

And please be aware that the duty of DCLKO.
The details, please refer the below.

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DCLKO Jitter

1. If the Clock comes from the internal PLL
Although it depend on stability of supplied power for PLL, reference values are as follow.

Coral -60ps to +60ps

2. If the Clock is given via DCLKI
If DCLKI does not include jitter, DCLKO does not include jitter also.

These specs assume that ideal input clock is given.

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Enable interrupts, IMASK register

There description in the hardware manual is wrong

Correct is IMASK:
1:Not mask
0:mask

Set the bit to 1 to enable the according interrupt.

By calling the function “GdcGeoSetInterruptMask” is the parameter set to the IMASK register.

e.g. enable command interrupt
GdcGeoSetInterruptMask (0x2);

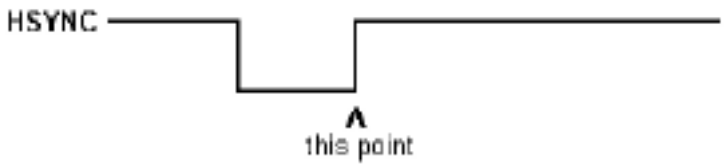
Q22: [back to top]
External synchronisation

FAQ – Coral LQ
External synchronous signal

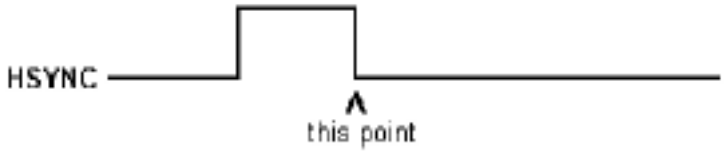
Coral detects the negative edge of the horizontal synchronous pulse from the external and synchronizes it.
The negative edge depends on the SF bit in the DCM register.

the negative edge means:

is SF active low -> rising edge of HSYNC
SF bit = 0 (negative logic)



is SF active high - falling edge of HSYNC
SF bit = 1(positive logic)



You need HSYNC and VSYNC only for the external synchronization, like it is described in the diagram for the external synchronization (the described EO pin is no longer used).

If you set ESY bit = 1 in the DCM/DCEM register and that way the external synchronization mode is set, you can connect HSYNC and VSYNC, independently of DEN='0'. There is no conflict. The display shouldn't be destroyed.

If the display is disabled, the levels for HSync/VSync are passive levels.
if SF-bit is low -> the synchronous signals are high
if SF-bit is high -> the synchronous signals are low

during the display is disabled.

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Differences between Coral P and Coral PA

- PCI bandwidth will increase to approx. 70MB/s
- Direct RGB666 video input without conversion to YUV422
- Current method still available as programmable option
- Brightness, Contrast, Saturation control for video input
- New ROM for Geometry Engine (enhanced float functions)
- Pixel-clock delay of display output is programmable : 180-deg shift and 2.5ns step shift
- PCI busclock can be used as clock input (additional mode)
- Enhanced Video texture mapping
- Enhanced Video up- and down-scaling
- Dual Display Output

14.09 Coral P/PA reset default levels

The default levels of the below signals after reset are:
digital RGB: output "0"
Pixel clock: output a clock divided by 1/62 of internal PLL
Hsync,Vsync: Hi-z (input mode)
DEN : output "0"

>>Do we need any pull-ups for any signal ?
Regarding this question, there is a description how to treat the
signals in the Coral-P manual, page 26, "2.2.3 Pin Treatment Table".

Q24: back to top
Converting 16bit ARGB to RGB888

For each color component, 3bit shift to MSB(left) is applied.
111 is filled at lower bits if a component is not zero.
000 is filled at lower bits if a componet is zero.