

FAQ list for MB86291 Scarlet and MB86292 Orchid

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History

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Graphic Controller frequently asked questions

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MB86291 SCARLET AND MB86292 ORCHID QUESTIONS :

Q1:
Is the Scarlet just a "Cremson + embedded SDRAM" ?

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No ! Scarlet is NOT just the combination of Cremson and SDRAM.
We should be aware about the following major functional upgrade
from Cremson to Scarlet:

(1) Full support geometry processor

Prior to the design of Cremson, our graphics team had participated to develop own geometry processor devices to be used in arcade game and PC graphics (all interactive 3D graphics operations). According to the market requirement to accelerate the total 3D graphics operation (not depending upon the host CPU's floating point computation power), we had determined to integrate

2 sets of Pinolites with enhanced rendering core into one silicon chip. These Pinolite units are to handle the entire 3D geometry process (transport, lighting, clipping, screen projection, triangle set up)

on behalf of host CPU at 1M polygons/sec of sustained performance. Therefore, even if the burden of the host CPU will be very high, due to all the other operation requirements, still fast enough

2D/3D operation is performed by the Rose/Scarlet.

(2) Digital video capture and flexible scaling

Video capturing feature was eliminated from Cremson at the very last minute due to the pin count limit. Now, because of the embedded SDRAM (no more external memory interface), we have enough pins to assign for digital video input and output. This new module is almost the same size as display control module of Cremson.

(3) Enhanced Pixel engine and memory interface bus width

Although Cremson offered only 800MBPS of memory bus band, Scarlet is capable to provide x2 band width. To make a best use of this bus band, drawing unit (DDA, pixel engine, Blt engine) as well as the memory interface unit were all enhanced, so that Rose/Scarlet can deliver x5 performance to Cremson.

Considering all the above factors :

Scarlet = 2xGeoProc + Enhanced Cremson (x5 performance) + Dedicated video capture/scaler + embedded SDRAM of wide bus band

Therefore the definition of Scarlet is not simply the addition of existing Cremson and conventional SDRAM devices. Please be aware about this many new function blocks are integrated to maximize the speed performance (x5 of performance of Cremson).

Q2:

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Is Orchid basically the same as Scarlet, but without embedded SDRAM ?

The major difference is in fact the SDRAM which is limited to 2 MB (16 Mbit) in the Scarlet device. For all applications which require more than 2 MB, the Orchid can be used. In this case up to 32MB of SDRAM and FCRAM can be connected. Another difference is the analog video output. The Orchid only has digital RGB and no DAC (Scarlet has both).

Q3:

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Is Scarlet&Orchid Software-compatible to Cremson ?

Yes. All the register areas and display list formats of the common functions are identical. The added functions like video input and geometry processors are separated. Software which was developed using the Cremson evaluation-board MB86290EB-01 can also be used with Scarlet. The only change that has to be made is to the memory mode register (MMR) - see the demos provided for details.

Also special care has to be taken in terms of the limited frame memory size.

Q4:

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Video Capture Unit of Scarlet&Orchid :
How can analog video signals be input to the interface ?

Scarlet&Orchid feature an ITU RBT656 (YUV 4:2:2) digital video interface. An external decoder such as Phillips UAA711x is required to convert the analog video signals to this digital format. The data stream will be read in from the Scarlet by the VI port and then written to graphics memory.

Analog processing, upsampling filters etc. are part of the external decoder. For details, see the application note about the video input unit of Scarlet !

Q5:

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Video Capture Unit of Scarlet&Orchid :
Can different video input and display frame rates be used ?

Yes, this is possible. The video input unit can asynchronously write to the frame grabber memory buffer and the circular buffer management will automatically duplicate or leave out frames in order to adjust to the display frame rate.

Can different video input and display resolutions be used ?

Yes, the part to be grabbed from the video stream can be selected using the registers CIHSTR, CIVSTR, CIHEND and CIVEND. The total size to be put in the frame memory is determined by CHP und CVP. The size and position of the picture to be finally displayed can be set by the register values of the W-layer which is dedicated for the video input module.

For details, see the application note about the video input unit of Scarlet !

Q6: [back to top](#)
Can the video input signal be mixed with information by alphablending?

Yes, for example it is possible to put text or graphics on the C-layer alphablended on top of the video (on W-layer).

Q7: [back to top](#)
There is a I2C interface implemented in Scarlet&Orchid.
On which pins is this interface located ?

The I2C pins of Scarlet are : 184 and 185
For details, see the I2C description of Scarlet !

Q8: [back to top](#)
Scarlet requires 14,32MHz (4* NTSC) input clock.
Is it possible to use another crystal (e.g.14,25MHz) ?
What is the allowed range of deviation (PLL) ?

The 14.25MHz as input clock is OK.
The allowed range of output frequency of PLL is around 195..202kHz.

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What is the weight (in grams) of the final Scarlet chip (mass production version) ?

The typical weight of HQFP208 package is 5.17g.
Errors of plus or minus several percent will arise.

Q10: [back to top](#)
Using SH-3 @ 66 Mhz together with Scarlet :
The "XRDY delay time" is specified with $t(RDYD)=7ns$ (max). In the Hitachi SH3-spec there is a value given for "Wait setup time" = 12ns (min) @ 66MHzoperation frequency. Under these worst case conditions, the wait line could eventually cause problems. Did your customers had problems with that ? Do you have any recommendations ?

We've assumed the max. frequency of SH3 bus-clock as 50MHz. If customer use higher frequency, they need to set the software wait to 3 cycle. We are now checking the behavior of this setting by logic simulation.

Q11: [back to top](#)
Is the load capacitance specified (C=16pF) valid for all ports of Scarlet ?

Yes, all the input load is same.

Q12:

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Power consumption figures and temperature of Scarlet :

Testcase: running 3D graphics demo for 10 minutes :

1. DAC Power down mode off (default)

1-1. Measurements

The Temperature of package : 47 degree

The Temperature of room(Ta): 25 degree

The current consumption : 630mA @VDDI-pin(2.5V)

6mA @VCC-pin(2.5V)

25mA @VDDE-pin(3.3V)

1-2. Estimates

The power consumption : 1.672W

A rise rate of package : 16 degree/W

The temperature of package : $25(Ta) + 1.672*16 = 51.752$ degree

$85(Ta) + 1.585*16 = 111.752$ degree

2. DAC Power down mode on

2-1. Measurements

The temperature of package : 47 degree

The Temperature of room(Ta): 25 degree

The current consumption : 595mA @VDDI-pin(2.5V)

6mA @VCC-pin(2.5V)

25mA @VDDE-pin(3.3V)

2-2. Estimates

The power consumption : 1.585W

A rise rate of package : 16 degree/W

The temperature of package : $25(Ta) + 1.585*16 = 50.36$ degree

$85(Ta) + 1.585*16 = 110.36$ degree

Q13:

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DAC power down mode :

If only the digital video interface is used for a digital display, is it possible for power consumption reduction to save the resistors at Vref-, AOUTR/B/G-, ACOMPB- and VRO-pin and leave them open or connect them to GND or Vcc (2.5V or 3.3V?) directly?

The DAC can be set in an undocumented "power down mode". To active this mode, write "0x00000001" to the register mapped at address "HostBase+0038h". In this mode, all analog pins can be connected to GND. Those pins are :
AVD, AVS, AOUTR, AOUTG, AOUTB, VREF, ACOMPR, ACOMPB, and VRO.

Q14:

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If CCLK and VI(0..7) at SCARLET are not used, what has to be done with them?

Please connect to GND.

Q15:

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There are two possible FCRAM-options mentioned in the Orchid-Manual :
16MBitx16Bit with 32bit databus or 64bit databus (4 or 8MByte). Can you please specify which available FCRAM devices can be connected (partnumbers)

SDR SDRAM type 16Mbit x16bit FCRAM
Parts number:MB81E161622
Orchid is able to connect 2 or 4 devices of that type .

Q16:

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What are the input limitations for the video input of Scarlet/Orchid ?

Scarlet or Orchid can accept variable formats under the limits shown below

max 720 pixels/raster
max 511 rasters/field
max 27MHz CCLK freq

Q17:

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How much is the decrease of drawing performance, while using AAF Feature ?

Anti-aliasing line's performance is 30-40 % of normal line's performance.

Q18:

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What can I do to make the Orchid chroma-key function work on the PCI board ?

Unfortunately, there are some hardware-bugs on the Orchid board which have to be fixed :

- 1) Polarity of clamp pulse (positive pulse must be given)
 - 2) Lack of load resistor at RGB output of LM1279A
(390ohm resistors must be connected between RGB out and GND)
 - 3) Over amplitude of DAC because of improper load in external sync mode. 75ohm load resistor should be added in parallel with existing 75ohm load.
 - 4) Noise
- If above problems are removed, then video level gets proper, but the signal might be noisy.

Q19:

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Recommendation for using the Orchid with the memory configuration:
2 x SDRAM 128MBit (x32) 64 bit bus width

Example type : MT48LC4M32B2TG

The following both connections are OK :

Orchid MA12 --> SDRAM BA1

Orchid MA13 --> SDRAM BA0

or

Orchid MA12 --> SDRAM BA0

Orchid MA13 --> SDRAM BA1

CKE connects to High(VDD).

CS connects to Low(GND).

For more details, please check the attached schematics and specifications.

Q20:

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How can I switch on/off the LEDs on the PCI board for testing ?

LEDs are memory mapped in the IO space. But the current map driver(mapdrv.dll) can not access the LED register which is mapped FPGA on the PCI board because this PCI map driver can access only 64MB.

The LED register is mapped 0x04001000 area.

So if you want to access the LED register, please use the "old" map driver (uty_cremson.dll).

sample code :

```
unsigned long FrameAddr;
```

```
if (GDC_FALSE==GdcInitialize()) return FALSE;
```

```
GdcSetMemoryMode(0x009a984a); //FCRAM 64Bit
```

```
GdcExecMode(GDC_DISABLE);
```

```
FrameAddr = Get_FrameAddress();
```

```
*((unsigned long *)(FrameAddr+0x4001000)) = 0x55555555;
```

Q21:

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What is the correct initialize routine for Scarlet ?

To initialize the Scarlet correctly, you have to follow these steps :

1. Hardware reset sequence :

after power-on, XRESET and S must be L to issue a reset S must be L for min 500ns
after S is H, XRESET must be held low for min 300us

2. After reset, we recommend to initialize the Scarlet in the following way (C language based):

```
// Initialize Scarlet
ret = GdcInitialize();          // init API
if (ret != GDC_TRUE) return;
GdcSetMemoryMode(0x003f3802);  // set MemoryMode
GdcSetInterruptMask(0xFF);    // mask interrupts
GdcExecMode(GDC_FALSE);       // set exec mode
```

on register level :

```
/* --MMR-- */
reg = (DWORD *) (HostBase + 0x0000fffc);
*reg = 0x003f3802;    /* SDRAM-Settings */

/* IMASK */
reg = (DWORD *) (HostBase + 0x00000024);
*reg = 0x0000001f;    /* 1f = all Interrupts to Host-CPU disabled */
```

Q22:

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using the Orchid (MB86292) we want to use a single 32-bit SDRAM from Micron (MT48LC4M32B2). Do the unused Data lines MD32-MD54 and MDQM4-7 need a pull up resistor to have a known state, or can I leave them open?

Please connect XRGBEN to Low (32-bit Bus Mode) so you can use all RGB Digital outputs R0-7,G0-7,B0-7. All other pins MD32-MD54 und MDQM4-7 can be left open.

Q23:

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How to connect the TESTx-pins ?

Scarlet - TESTL0, TESTL1, TESTH0, TESTH2, TESTH2, TESTH4 pins
Hardware manual page 16: 'TEST signals must be clamped to high level'.

The description of page16 is wrong.
Connect these pins same as eva-board.

TESTLx = GND; TESTHx = VDD3 (+ resistor).

Q24:
DCLKO Jitter @ Scarlet

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1. If the Clock comes from the internal PLL
Although it depends on stability of supplied power for PLL, reference values are as follow.

Cremson/Scarlet -150ps to +180ps

2. If the Clock is given via DCLKI
If DCLKI does not include jitter, DCLKO does not include jitter also.

These specs assume that ideal input clock is given.

Q25:
bank interleave

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Use bank interleave
(mapping the each layer to allocate the different bank)

If you use two pcs of x16bit, 4bank, 64Mbits SDRAM
(total 16MByte graphics memory), the banks are mapped like the below.

0x00000000-0x001fffff:bank 0
0x00200000-0x003fffff:bank 1
0x00400000-0x005fffff:bank 2
0x00600000-0x007fffff:bank 3

Then if you map each layer as the below, it is "the bank interleave".

0x00000000-0x001fffff:bank 0 => B-layer
0x00200000-0x003fffff:bank 1 => M-layer
0x00400000-0x005fffff:bank 2 => W-layer
0x00600000-0x007fffff:bank 3 => C-Layer

Q26:
Enable interrupts, IMASK register

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There description in the hardware manual is wrong

Correct is IMASK:
1:Not mask
0:mask

Set the bit to 1 to enable the according interrupt.

By calling the function "GdcGeoSetInterruptMask" the parameter is set to the IMASK register.

e.g. enable command interrupt
GdcGeoSetInterruptMask (0x2);