

# Errata Sheet MB88F332 Indigo

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## History

Date	Author	Version	Comment
14.03.2008	AvT	1.00	First release, Spec. 0.92 corrections
17.03.2008	AvT	1.10	Correction pins 149 & 152
31.03.2008	MN	1.20	Spec. 0.93 correction pins
04.07.2008	AvT	1.30	Added issues E2, E3, E4
30.07.2008	AvT	1.40	Added issue E5
07.01.2009	AvT	1.50	Added issues E6, E7
20.01.2009	AvT	1.60	Added ES3, modified text of E6, E7. Added correct chip part numbers for different ES types.
14.05.2009	AvT	1.70	Added E8, E9
10.07.2009	AvT	1.71	Modified E9 text and diagram
13.07.2009	AvT	1.72	Added small note to E9

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Errata List:

July 10th, 2009

No	Item	Effected samples		
		ES1* DC: 0822	ES2** DC: 0845	ES3*** DC: 0913
		DC : available beginning with date code xxxx X : effected --- : not effected		
<a href="#">E1</a>	Hardware Manual Pin List Corrections	-	-	-
<a href="#">E2</a>	Stepper Motor Control drive limitation	X	-	-
<a href="#">E3</a>	RGB color channel mismatch	X	-	-
<a href="#">E4</a>	Operating conditions	X	-	-
<a href="#">E5</a>	Display background blend error	X	-	-
<a href="#">E6</a>	Line jitter in external synchronization mode	X	X	-
<a href="#">E7</a>	Instable reset operation	X	X	-
<a href="#">E8</a>	Signature Unit: Signature B: 'Summation Signature (pixel color values) limited for evaluation window covering column 0	X	?	X
<a href="#">E9</a>	Limitation of Signature Generation Unit (SIG)	X	?	X

- \* ES1: MB88F332AA (with APIX) / MB88F332AB (without APIX)
- \*\* ES2: MB88F332BA (with APIX) / MB88F332BB (without APIX).
- \*\*\* ES3: MB88F332CA (with APIX) / MB88F332CB (without APIX)

**Detail**

The Hardware Manual (specification) rev.0.93 contains errors in the pin list.

Pin No.	Rev. 0.93 [Error]	Rev. 0.94 [Correction]	Modification reason	Effect of applying to the specification (rev.0.93)
55	GPIO[3]/INT[3]	HOST_DI	PKG Assembly issue	changed function
56	GPIO[4]/INT[4]	HOST_DO	PKG Assembly issue	Bus conflict, high current
57	HOST_DI	HOST_INT	PKG Assembly issue	Bus conflict, high current
58	HOST_DO	HOST_SCK	PKG Assembly issue	Bus conflict, high current
59	HOST_INT	HOST_XCS	PKG Assembly issue	changed function
60	HOST_SC K	VDDI	PKG Assembly issue	Short circuit
61	HOST_XCS	VSS	PKG Assembly issue	Short circuit
62	VDDI	VD5	PKG Assembly issue	Short circuit
63	VSS	APIX_CNFG[2]	PKG Assembly issue	changed function
64	VD5	APIX_CNFG[1]	PKG Assembly issue	Short circuit
65	APIX_CNFG[2]	XTAL1	PKG Assembly issue	changed function
66	APIX_CNFG[1]	XTAL0	PKG Assembly issue	changed function
67	XTAL1	VSS	PKG Assembly issue	Short circuit
68	XTAL0	RREF	PKG Assembly issue	Short circuit
69	VSS	VSSA0	PKG Assembly issue	changed function
70	RREF	SDOUTP	PKG Assembly issue	changed function
71	VSSA0	SDOUTM	PKG Assembly issue	changed function
72	SDOUTP	VSSA1	PKG Assembly issue	changed function
73	SDOUTM	VDDA0	PKG Assembly issue	changed function
74	VSSA1	SDINP	PKG Assembly issue	changed function
75	VDDA0	VCM	PKG Assembly issue	changed function
76	SDINP	SDINM	PKG Assembly issue	changed function
77	VCM	VDDA1	PKG Assembly issue	changed function
78	SDINM	APIX_CNFG[0]	PKG Assembly issue	changed function
79	VDDA1	GPIO[3]/INT[3]	PKG Assembly issue	changed function
80	APIX_CNFG[0]	GPIO[4]/INT[4]	PKG Assembly issue	changed function
105	NC	VDD_RSDS[0]	PKG Assembly issue	Short circuit
106	NC	VDDI	PKG Assembly issue	Short circuit
107	VDD_RSDS[0]	VSS	PKG Assembly issue	Short circuit
108	VDDI	DISPP[0]	PKG Assembly issue	Short circuit
109	VSS	DISPN[0]	PKG Assembly issue	Short circuit
110	DISPP[0]	VDD_RSDS[1]	PKG Assembly issue	changed function
111	DISPN[0]	DISPP[1]	PKG Assembly issue	changed function
112	VDD_RSDS[1]	DISPN[1]	PKG Assembly issue	Short circuit
113	DISPP[1]	VSS	PKG Assembly issue	changed function
114	DISPN[1]	DISPP[2]	PKG Assembly issue	changed function
115	VSS	DISPN[2]	PKG Assembly issue	Short circuit
116	DISPP[2]	VDDI	PKG Assembly issue	changed function
117	DISPN[2]	DISPP[3]	PKG Assembly issue	changed function
118	VDDI	DISPN[3]	PKG Assembly issue	Short circuit
119	DISPP[3]	VSS	PKG Assembly issue	changed function
120	DISPN[3]	DISPP[4]	PKG Assembly issue	changed function
121	VSS	DISPN[4]	PKG Assembly issue	Short circuit
122	DISPP[4]	VDD_RSDS[2]	PKG Assembly issue	changed function
123	DISPN[4]	DISPP[5]	PKG Assembly issue	changed function
124	VDD_RSDS[2]	DISPN[5]	PKG Assembly issue	Short circuit
125	DISPP[5]	VSS	PKG Assembly issue	changed function
126	DISPN[5]	DISPP[6]	PKG Assembly issue	changed function
127	VSS	DISPN[6]	PKG Assembly issue	Short circuit
128	DISPP[6]	VDDI	PKG Assembly issue	changed function
129	DISPN[6]	DISPP[7]	PKG Assembly issue	changed function

130	VDDI	NC	PKG Assembly issue	changed function
131	DISPP[7]	DISPN[7]	PKG Assembly issue	changed function
132	DISPN[7]	VSS	PKG Assembly issue	changed function
133	VSS	DISPP[8]	PKG Assembly issue	Short circuit
134	DISPP[8]	DISPN[8]	PKG Assembly issue	changed function
135	DISPN[8]	VDD_RSDS[3]	PKG Assembly issue	changed function
136	VDD_RSDS[3]	NC	PKG Assembly issue	changed function
143	FLSH_DI	NC	PKG Assembly issue	changed function
144	FLSH_DO	FLSH_DI	PKG Assembly issue	Bus conflict, high current
145	FLSH_SCK	FLSH_DO	PKG Assembly issue	changed function
146	FLSH_XCS	FLSH_SCK	PKG Assembly issue	changed function
147	TCON_TSIG[0]	FLSH_XCS	PKG Assembly issue	changed function
148	TCON_TSIG[1]	TCON_TSIG[0]	PKG Assembly issue	changed function
149	VDDE	TCON_TSIG[1]	PKG Assembly issue	Short circuit
150	VSS	VDDE	PKG Assembly issue	Short circuit
151	VDDI	VSS	PKG Assembly issue	Short circuit
152	TCON_TSIG[2]	VDDI	PKG Assembly issue	changed function
153	TCON_TSIG[3]	TCON_TSIG[2]	PKG Assembly issue	changed function
154	TCON_TSIG[4]	TCON_TSIG[3]	PKG Assembly issue	changed function
155	TCON_TSIG[5]	TCON_TSIG[4]	PKG Assembly issue	changed function
156	NC	TCON_TSIG[5]	PKG Assembly issue	Short circuit

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E2:  
Stepper Motor Control drive limitation

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#### Detail

The maximum driving (current) of the SMC pins is limited to 5mA (the intended maximum driving current is 30 mA).

**Warning:** Drawing more current than 5mA via a direct connection to stepper motors will reduce the lifetime of the GDC. Furthermore, the full voltage output level might not be fully reached and there will be a side effect on EMI performance.

#### Workaround:

Use external driver IC's in your PCB design until ES2 is available.

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E3:  
RGB color channel mismatch

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**Detail**

The RGB color channel assignments of MB88F332 'Indigo' GDC are not compliant with the APIX standard (effects APIX pixel link only!)

	<i>MB88F332</i>	<i>APIX</i>
18bpp	px_data[17:12] -> Red Data[5:0]	px_data[17:12] -> Blue Data[5:0]
	px_data[11: 6] -> Green Data[5:0]	px_data[11: 6] -> Green Data[5:0]
	px_data[ 5: 0] -> Blue Data[5:0]	px_data[ 5: 0] -> Red Data[5:0]
24bpp	px_data[23:16] -> Red Data[7:0]	px_data[23:16] -> Blue Data[7:0]
	px_data[15: 8] -> Green Data[7:0]	px_data[15: 8] -> Green Data[7:0]
	px_data[ 7: 0] -> Blue Data[7:0]	px_data[ 7: 0] -> Red Data[7:0]

**Workaround:**

Workarounds may be possible depending on the specific application use case. It is not possible to make a global statement which can be guaranteed at this time. Please contact the Application Engineering group at: [gcc\\_info@fme.fujitsu.com](mailto:gcc_info@fme.fujitsu.com) for support.

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E4:  
Operating conditions

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**Detail**

The correct operation of the MB88F332 is currently only guaranteed under the following conditions:

Voltage: 1.8V..1.95V  
Temperature: -40..+50 deg.

For your information, the specified operating range conditions are:  
Voltage: 1.65V..1.95V  
Temperature: -40..+125 deg.

**Workaround:**

Use limited operating conditions stated above.

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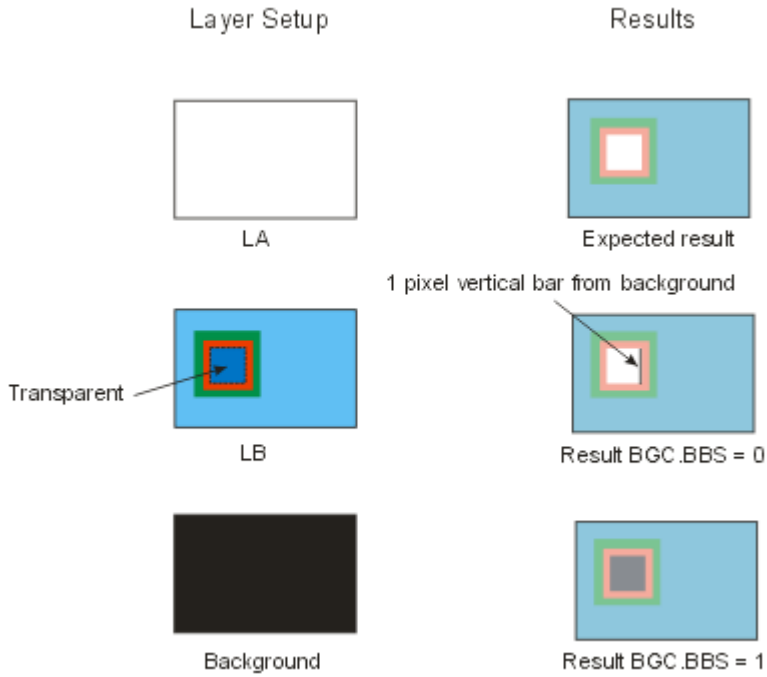
E5:  
Display background blend error

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**Detail**

When the Video Display Controller is set up with LA on top of LB with blending in LA [LABLD], and transparency in LB [LBETC], e.g.

(Top)  
LA Layer (white, with alpha blending)  
LB Layer – (with a sprite and using a transparent color)  
Background Layer (black)  
(Bottom)



and background color blending is disabled (Background Color register [BGC], bit BBS=0), the pixels with the transparent color will show a 1-pixel wide bar with the background color on the righthand side. The same occurs if the ordering and roles of LA and LB are exchanged.

**Workaround:**

There is no workaround for this problem. However, the issue does not occur when background color blending is enabled (Display Background Color register [BGC], bit BBS=1).

**Detail**

Panel output is affected by line jitter if the display controller module is used in the 'external synchronization' mode and the TCON module is simultaneously active (i.e. TCON bypass is disabled). Panel timing parameters such as horizontal back porch show a jitter of +/- 1 pixel clock period. Please note that although the jitter is physically present, it may not be visible if a panel is used that has an internal TCON (or similar logic circuitry). This is because some TCONs are able to compensate the jitter of the incoming H-sync by also evaluating the DE (Data Enable) signal.

**Workaround:**

The concept behind the following workaround is to shift the h-sync pulse to a more suitable region that is not effected by jittering.

Insert dummy columns on the lefthand side of the active display area. As a consequence, all sprite coordinates or external graphic layers must be shifted to the right.

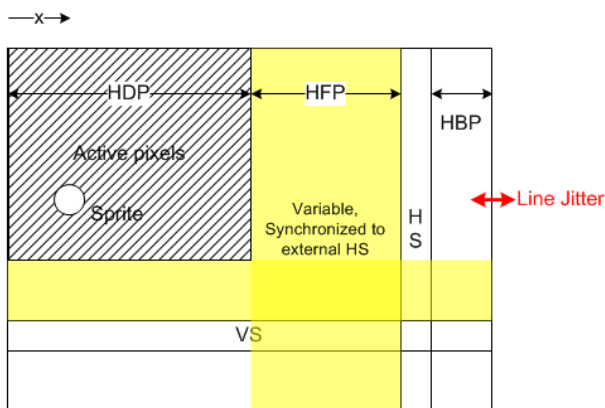
The horizontal coordinates of the TSIG module pulse generators (which influence the horizontal backporch) can now be programmed according the following equation:

$$0 \leq x < HDP$$

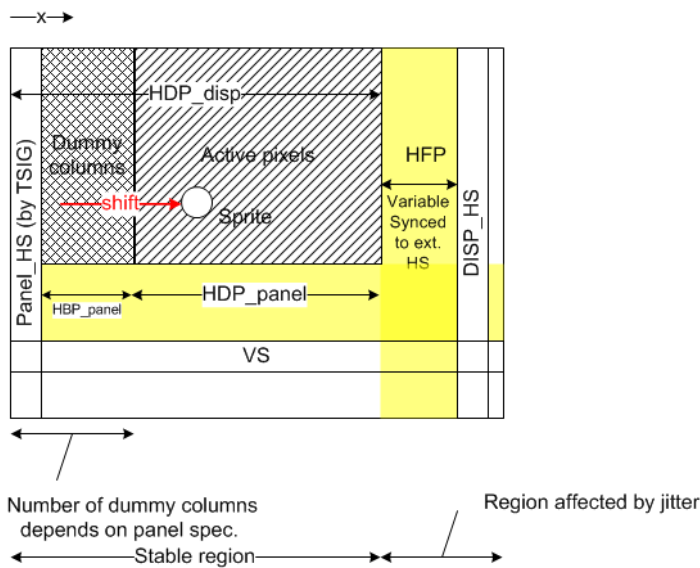
This generates a stable horizontal back porch.

The following two diagrams serve to clarify the problem and its workaround.

**Current Situation**



## Software Workaround



E7:  
Instable reset operation

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### Detail

It is possible that the internal power-on reset is not reliable.  
(Hint: internal power-on reset is activated by mode pin `RSTB_MODE[1] = 0`)

### Workaround:

Deactivate the internal power-on reset by setting mode pin `RSTB_MODE[1] = 1`.  
Apply a reset pulse (duration 8ms or more) to the external pin `XRST` by using e.g. RC circuitry.

E8: [back to top](#)  
Signature Unit: Signature B: 'Summation Signature (pixel color values) limited for evaluation window covering column 0

### Detail

For the checksum type Signature B: 'Summation Signature' (pixel color values), the checksum is not reset at the end of the frame if the left evaluation window column is column 0.

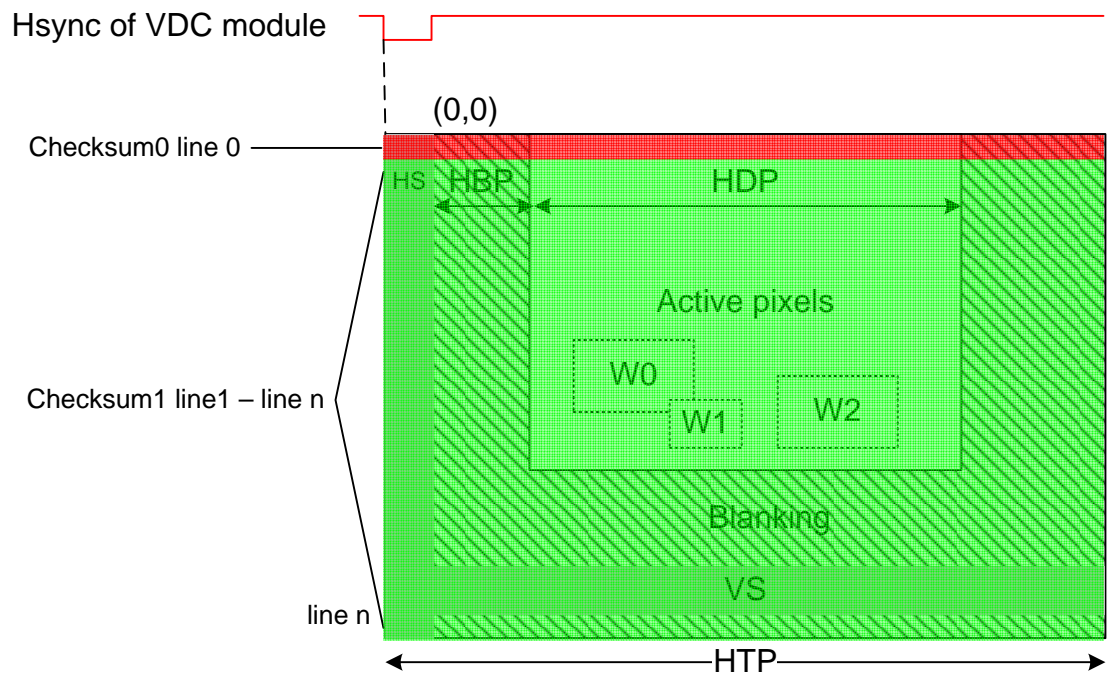
This means that the SIG unit register `HorizontalUpperLeftW0` may not be set to 0.

### Workaround:

Set `HorizontalUpperLeftW0` to values  $>0$ .

**Detail**

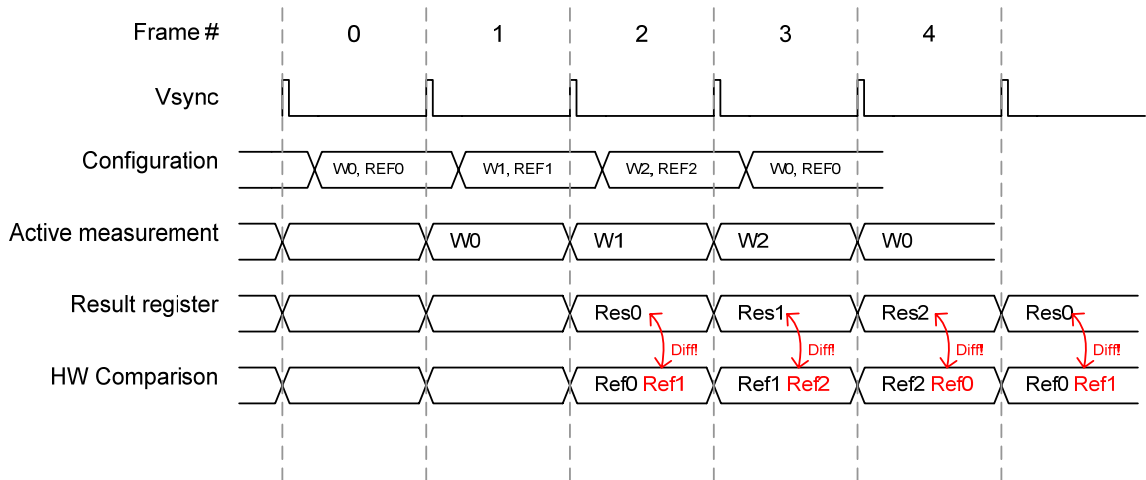
Two checksums (instead of one) are generated per frame; one covering line 0, the other from line 1 to line n (n = content of the display controller Vertical Total Raster register 'VTR' + 1). The result registers show only the result of line 0.  
Consequence: The content of line 1 to n can not be monitored directly by an external microcontroller using the result registers Signature[A|B][R|G|B]W0.



The continuous monitoring of multiple windows with different coordinates is not possible in the way described in the Hardware Manual.

The following diagram shows (in black) the specified behaviour, whereas the red color illustrates the current behavior of the chip.

- Wi : Co-ordinates of Evaluation Window i
- REFi : Reference values of Evaluation Window i
- RESi: Result values of Evaluation Window i



**Figure 1 - Example for cyclic monitoring of 3 windows**

**Workaround:**

Do not use an evaluation window which covers line 0.

The vertical co-ordinates (Registers Vertical\* ) of the evaluation window of Checksum1 (green area) must be set to line number - 1. The same is valid for the mask Registers MaskVertical\*.

Use the built-in, automatic comparison mechanism with reference checksums, i.e. program the registers covering the reference values (Registers Sign[A|B]Reference[R|G|B|W0]).

Use the continuous checksum generation mode (Register TriggerW0.TrigMode=01b)

The comparison mechanism will now detect (for every frame) a mismatch of the Checksum0 (covering line 0) and a match for Checksum1 (covering line 1 to line n).

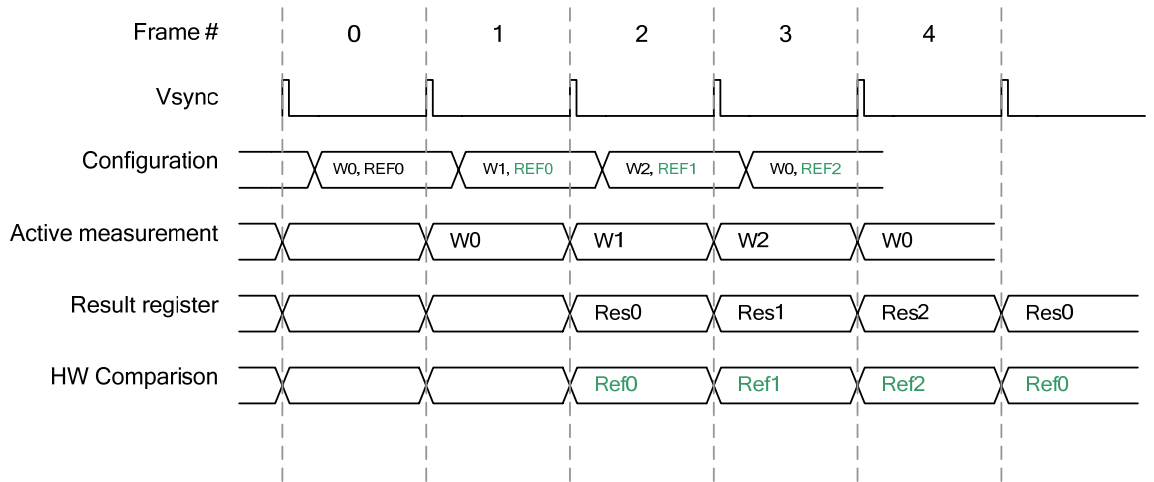
If therefore, the mechanism for resetting the error counter is used (Register ErrorThreshold.ErrThresReset=1), a read of the error counter (Register Signature\_error.Sig\_error\_count) constantly shows a 1.

To generate an interrupt after 3 frames with failing checksums (line 1 - line n), set the register ErrorThreshold.ErrThres = 6.

To support continuous monitoring of multiple windows with different coordinates program the reference values one frame delayed relative to their respective window coordinates setup. This shifted programming of reference values is shown in the following diagram.

**Note:**

This workaround is a suggestion. Other solutions may be feasible, depending on your application. For details in specific cases, please contact [gdc\\_tech\\_support@fme.fujitsu.com](mailto:gdc_tech_support@fme.fujitsu.com)



**Figure 2 - Shifted programming of reference values**