Errata Sheet MB86296 Coral PA

History

Date	Author	Version	Comment
5.08.2004	AG	1.0	First release
27/10/2005	AG	1.1	Issue E12 added

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Errata List:

October 28th, 2005

number	Item
E1	register access fails, if PCI pre-fetch is running (only ES sample)
E2	Reading the BST (burst status) register fails during burst transfer (only ES sample)
E3	PCI performance is not speeded up in burst read mode (only ES sample)
E4	Retrying the read access fails if Coral is write accessed (only ES- sample)
E5	C/BE hangs up (only ES sample)
E6	Multi master access fails (only ES sample)
E7	Access to host register area fails after video memory is write accessed (only ES sample)
E8	Failed data on 1CLOCK or less of the IDLE phase (only ES sample)
E9	VRAM - HST register boundary burst read hang-up
E10	Burst complete flag does NOT set in burst size = "1" and Slave read
E11	Can NOT transfer correctly between Coral and the device which does NOT support to issue the odd starting address
E12	Multi master access and local DMA

E1: back to top
register access fails, if PCI pre-fetch is running (only ES sample)

Detail
During the “pre-fetch module” is working, if master tries to access the Coral-PA registers(other than memory), that access does NOT work correctly.

Cause:
The “pre-fetch module” was implemented to speed-up the burst memory read.
This module read and store the next address data to the internal buffer after read the memory. And reply this buffer data when the next reading address is same as buffered address.
But if the master try to access the Coral-PA’s registers during this pre-fetch module is working, this master access conflicts pre-fetch read and failed register access.

Workaround:
this problem occurs only with ES-sample, it will be corrected before mass production

E2: back to top
Reading BST (burst status) register fails during burst transfer is active (only ES sample)

Detail
During the burst transfer, if master tries to read the BST registers(HostBase+0x8040), the Coral does NOT reply the read data.(Retry forever)

Workaround:
this problem occurs only with ES-sample, it will be corrected before mass production

E3: back to top
PCI performance is not speeded up in burst read mode (only ES sample)

Detail
If register location is changed from 0x1fc0000-0x01ffffff to 0x3fc0000-0x3ffffff by RSW register, the burst read performance is not speed-up in the area 0x1fc0000-0x1ffffff.

Workaround:
this problem occurs only with ES-sample, it will be corrected before mass production

E4: back to top
Retrying the read access fails if Coral is write accessed (only ES- sample)

Detail
If write access comes to Coral during the read retry, this read access return the retry forever.

Workaround:
this problem occurs only with ES-sample, it will be corrected before mass production

E5: back to top
C/BE hangs up (only ES sample)

Detail
If read access other than CBE code=0x0110 comes to Coral-PA continiusly, this read access return the retry forever.

Workaround:
this problem occurs only with ES-sample, it will be corrected before mass production

E6: back to top
Multi master access fails (only ES sample)

Detail
If write access comes to Coral during the read retry, this read access return the retry forever.
The phenomen is acutally same as “E4”.

Workaround:
this problem occurs only with ES-sample, it will be corrected before mass production

E7: back to top

Access to host register area fails after video memory is write accessed (only ES sample)

Detail

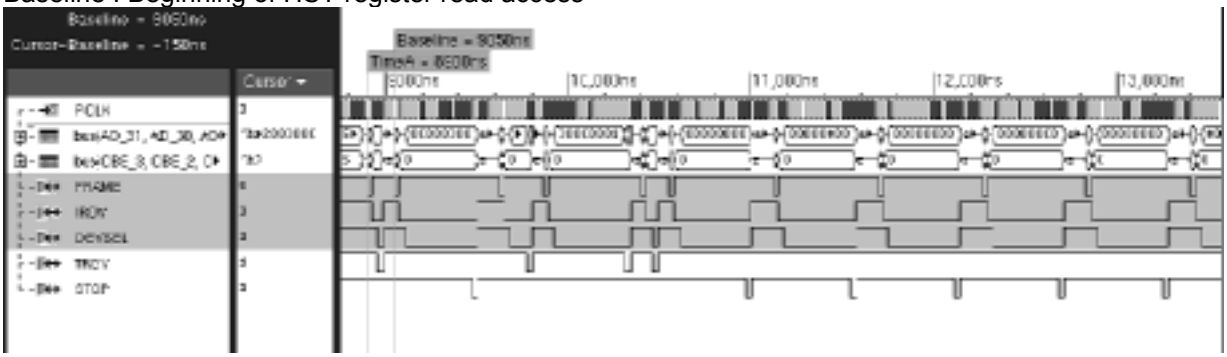
If the CPU accesses the HST register(0x1fc0000-0x1fc00f0) following the VRAM write access as shown in the Figure1, the PCI is hanged up. As the example, while it writes the display list in the VRAM in continuity, the CPU read the IST register by the handler of the interrupt, the the PCI is hanged up.

Cause:

If the CPU accesses the HST register on the condition that the VRAM write access is waiting internally, the internal state goes wrong.

TimeA : Beginning of VRAM write access

Baseline : Beginning of HST register read access



Workaround:

this problem occurs only with ES-sample, it will be corrected before mass production

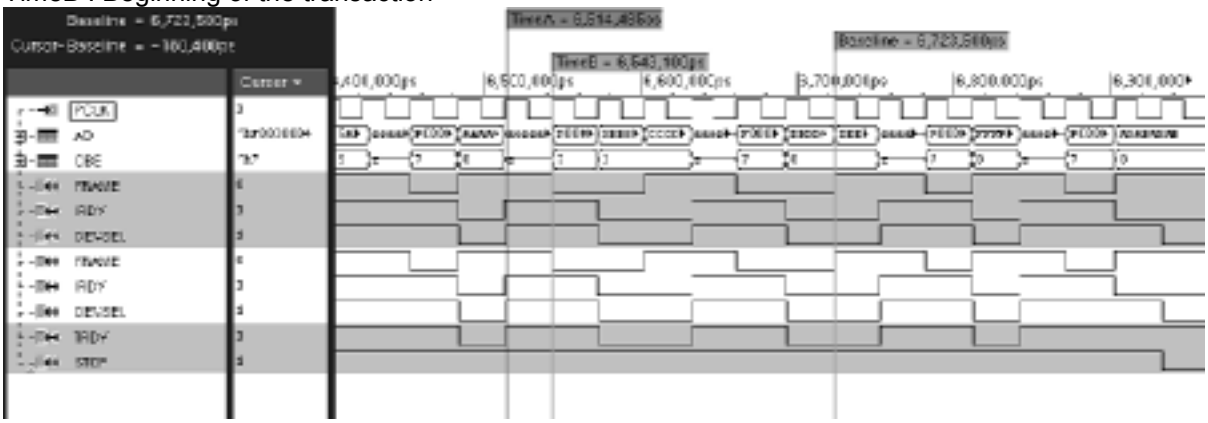
E8: back to top
Failed data on 1CLOCK or less of the IDLE phase (only ES sample)

Detail
The data is garbled, when the IDLE phase of the write transaction is 1 or less CLOCK cycle (The period between TimeA and TimeB is 1CLOCK cycle as shown the Figure1).

Cause:
The retrial termination is not performed by asserting the STOP signal by the Baseline clock.

Measure:
PA : We will modify the logic of PA.
Modifing the logic, Coral-PA will accept 1 clock of the IDLE phase.
But still don't accept 0 clock of the IDLE phase(= This protocol called "fast write to back")
Therefore don't access the Coral-PA in fast write to back protocol.
LP : -

TimeA : Termination of the transaction
TimeB : Beginning of the transaction



Workaround:
this problem occurs only with ES-sample, it will be corrected before mass production

E9: back to top
VRAM - HST register boundary burst read hang-up

Detail
If master access the Coral from VRAM to HST registers continuity by burst read, the register read replies the retry forever.

Workaround:
PA : Don't burst read from VRAM to HST continuity.
Ex.)Burst size=8, don't read 1fbffe4-1fbfffc

E10: back to top
Burst complete flag does NOT set in burst size = "1" and Slave read

Detail
In case of slave read and burst size=”1”, burst complete flag in IIST and BST register does NOT set.

Workaround:
PA : Don't set burst size to "1" in Slave read using BCU

E11: back to top

Can NOT transfer correctly between Coral and the device which does NOT support to issue the odd starting address

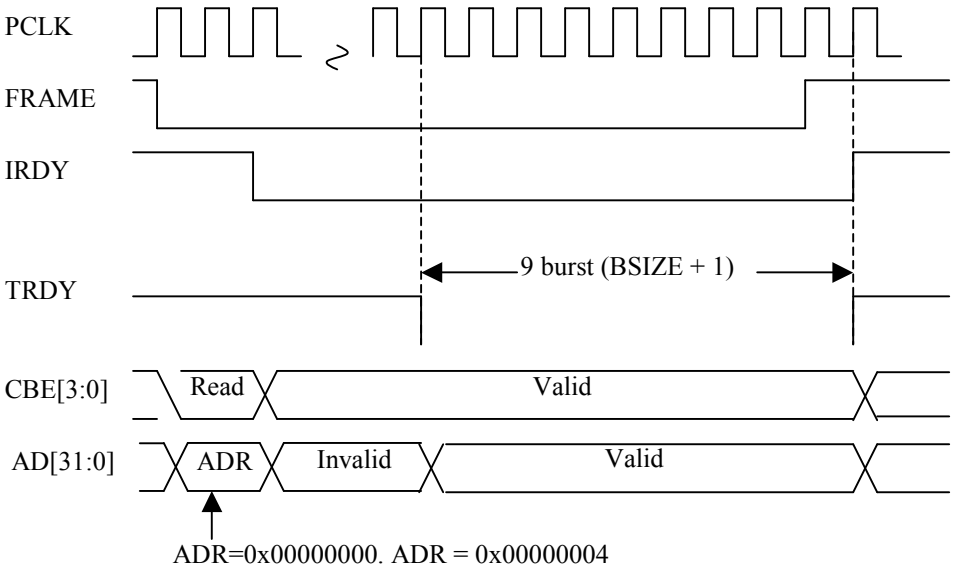
Detail

11-1. Coral = PCI Master.

Coral can't issue an odd address to PCI area.
If Coral is the master device and the beginning address is set to the odd address in 64-bit boundary, Coral issue the previous even address.
Note: The odd address in 64 bit boundary means 0x04, 0xC.

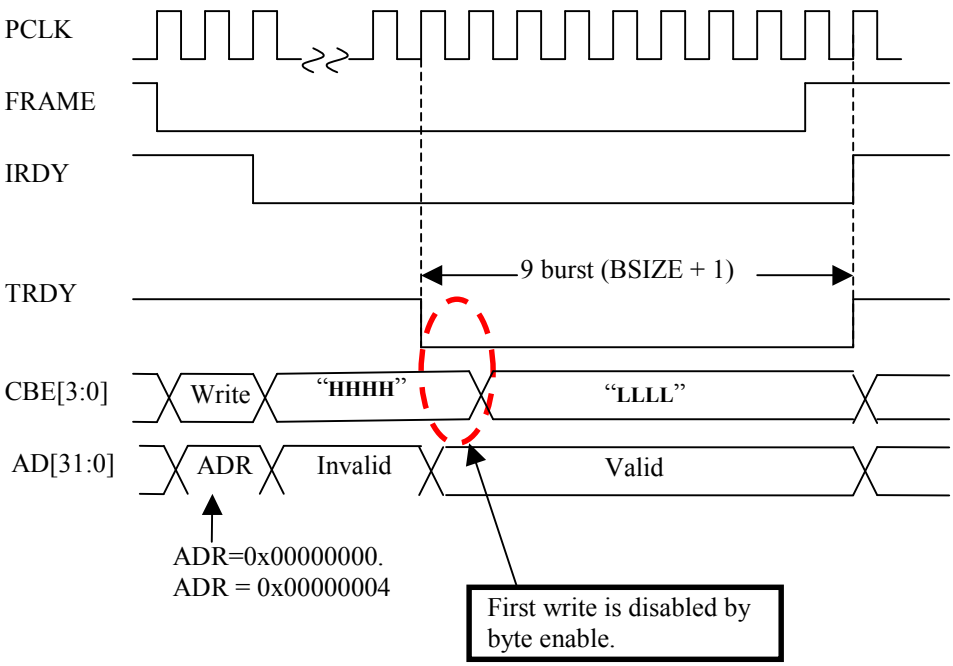
In Coral master read mode, Coral begins to read the previous even address and read the setting of burst size(BSIZE of BCR) plus "1".

Ex. Source address=0x00000004, BSIZE of BCR = 8,



In **Coral master write mode**, Coral begins to write the previous even address with disable write byte enable and write the setting of burst size(BSIZE of BCR) plus “1”.

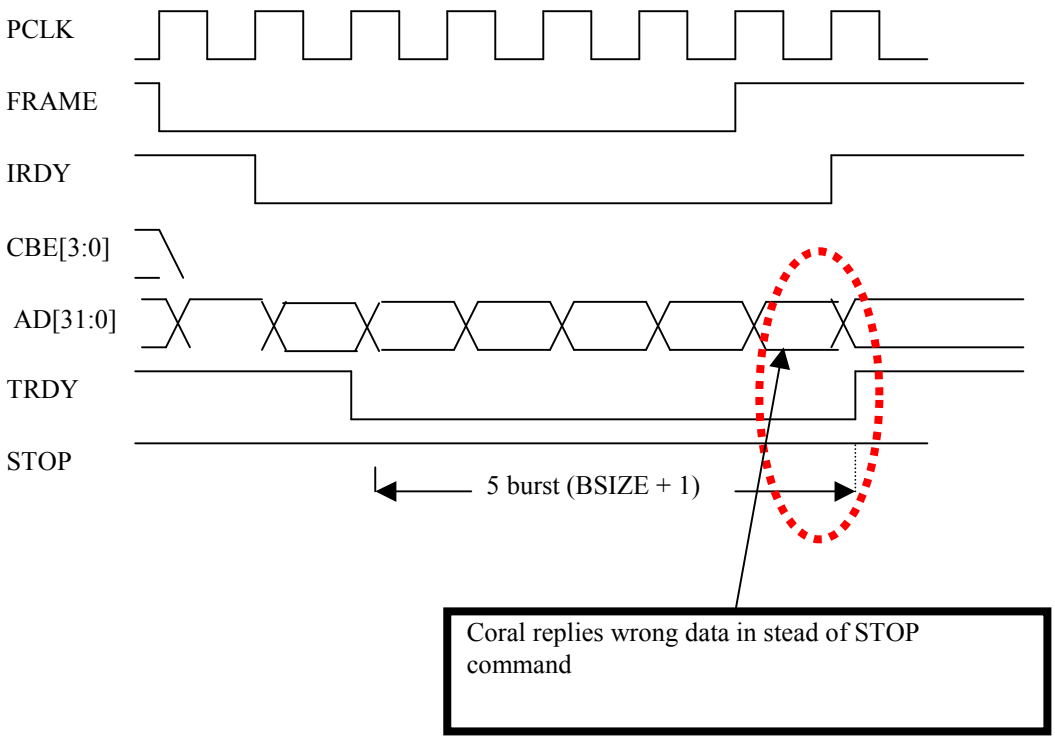
Ex. Source address=0x00000004, BSIZE of BCR = 8,



11-2. Coral = PCI Slave.
Phenomenon:
Coral reply the wrong data, if the read burst size comes more than the setting of SRBS.
This phenomenon occurs only burst read.
In burst write, Coral is able to issue the STOP command if there is no more available internal buffer.

Detail:
Coral replies the retry until storing the SRBS size data to Coral's PCI internal buffer.
After stored the data, Coral begins to reply the data by TRDY. But if the burst read comes more than the size of SBRS, Coral replies the wrong data instead of issuing the STOP.

Ex. BSIZE of BCR = 4, Master issues the **burst read** more than "BSIZE+1" from Coral.



E12:
Multi master access and local DMA

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The Coral can fail in case of multi master access and a local DMA are running at the same time.

(a) Conditions:
(1) Two PCI masters access Coral-PA via PCI bus. One master (Master-A) writes data to the memory which connected to Coral-PA. Another master (Master-B) reads data from the Coral-PA. These two transactions are executed independently and simultaneously. The problem does not occur, if both master are reading or writing to the Coral.
(2) The “Local Display List” transfer and rendering operation are initiated at the same time.

(b) phenomenon
Because of the two independent data transfer from PCI master-A and B, it happens that write transaction from master-A occurs just after RETRY response of PCI from Coral-PA for the preceding read transaction of master-B. In certain condition of internal timing of Coral-PA among above transaction occurring, the write transaction by Master-A fails as the phenomenon that the data is written to different address intended (wrong address is used for the write transaction). In this problem, the wrong address value was swapped from the series of the data originally intended to store the memory. Therefore, the value of the wrong address is random value in general.
This problem occurs only in case the “Local Display List” transfer is initiated at the same time.

(b) workaround:
The access to the Coral must be synchronised.
Local DMA and multi master access may not occur at the same time. A single master access during a local DMA is running does not evoke the problem.

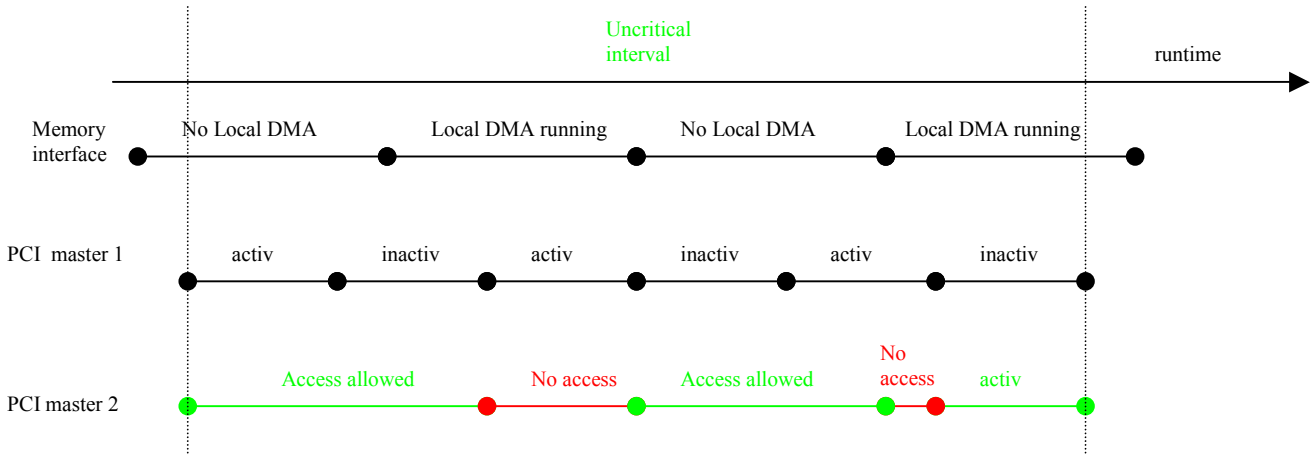

Figure 1 synchronising the access to the Coral