



Errata Sheet MB86295 Coral P

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History

Date	Author	Versio n	Comment
08.10.2003	AG	1.0	First release
Oct. 15 th , 2003	AG	1.01	I2C bug added
Feb. 20 th , 2004	AG	1.03	Problem by video capturing with up-scaling
Aug. 5 th , 2004	AG	1.04	PCI problems added
01.11.2005	AG	1.05	Multi master access and local DMA
02.01.2006	AG	1.06	Problem with video layer

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E1:
Texture Drawing with Stencil

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Detail

Draw a texture object with "stencil" in texture alpha blend mode.
After that, if you draw an alpha blend or anti-alias object without texture, the drawing does not work correctly.

Measure

Please use one of the following methods.

1) Please use "stencil alpha" with alpha blending ratio "0xff" in stead of "stencil".
There is no performance fall by this method.

2) After drawing a texture object with "stencil", please draw a texture object without "stencil" in texture alpha blend mode.

E2:
BltCopyAltAlphaBlendP command

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Detail

BltCopyAltAlphaBlendP command does not work correctly, after anti-aliasing line drawing.
If you draw a point or a line without anti-aliasing or a polygon(triagnle) before BltCopyAltAlphaBlendP command,
BltCopyAltAlphaBlendP command works correctly.

Measure

Please draw a point outside of clipframe before BltCopyAltAlphaBlendP command.

E3:
The texture mapping with bi-linear high-speed mode

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Detail

If you set the texture mapping with bi-linear high-speed mode, Coral-LP works as texture mapping with bi-linear normal mode.

Measure

Please use texture mapping with bi-linear normal mode.

E4:
Accessing the I2C interface registers(MB86295 only)

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Detail

If CPU tries to read or write the I2C registers during all of the burst transfer(include local transfer), the GDC does NOT reply TRDY signal.
This means the system is hung-up.

Measure

Don't read or write I2C registers during the burst transfer.
Check the transfer status by bit 23-0 of BST(HostBase+8014) before read or write I2C registers.

E5:
Problem by video capturing with up-scaling

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Detail

In a video capture Up-scaling function, there is a case where a video capture is not started even if it turns ON a video capture.

Measure

ON or OFF of a video capture (write to VIE and CM bits of VCM register) is synchronized with VSYNC interruption.

After detecting VSYNC interruption, the permission time to Captures ON or OFF is calculated by the below formula.
 $(HTP+1) * (VTR-VDP-4) - (HTP-HDP)$

The case of typical resolution is shown in the following.

Resolution	The permission time to Captures OF or OFF after interruption detection [msec]
1024 x 768	0.70
800 x 600	0.76
854 x 480	1.30
640 x 480	1.30
1280 x 1024	1.02

*note1 Capture ON:(VIE=1,CM=11) OFF:(VIE=0,CM=00)

*note2 This phenomenon is occurred only up-scaling.

E6:
Multi master access fails (only ES sample)

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Detail

If write access comes to Coral during the read retry, this read access return the retry forever. The phenomenon is acutally same as “E4”.

Workaround:

Don't write to registers or video memory during the retry.

E7:
Access to host register area fails after video memory is write accessed (only ES sample)

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Detail

If the CPU accesses the HST register(0x1fc0000-0x1fc00f0) following the VRAM write access as shown in the Figure1, the PCI is hanged up. As the example, while it writes the display list in the VRAM in continuity, the CPU read the IST register by the handler of the interrupt, the the PCI is hanged up.

Cause:

If the CPU accesses the HST register on the condition that the VRAM write access is waiting internally, the internal state goes wrong.

TimeA : Beginning of VRAM write access
Baseline : Beginning of HST register read access



Workaround:

Read video memory before reading the host register

E8:
VRAM - HST register boundary burst read hang-up

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Detail

If master access the Coral from VRAM to HST registers continuity by burst read, the register read replies the retry forever.

Workaround:

PA : Don't burst read from VRAM to HST continuity.
Ex.)Burst size=8, don't read 1fbffe4-1fbffc

E9:
Burst complete flag does NOT set in burst size = "1" and Slave read

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Detail

In case of slave read and burst size="1", burst complete flag in IIST and BST register does NOT set.

Workaround:

Don't set burst size to "1" in Slave read using BCU

E10:

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Can NOT transfer correctly between Coral and the device which does NOT support to issue the odd starting address

Detail

15-1. Coral = PCI Master.

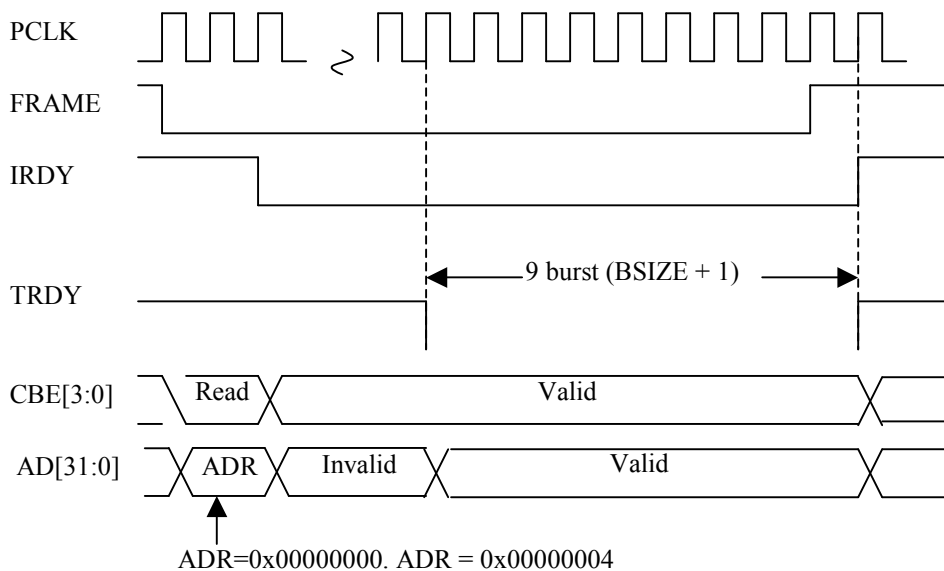
Coral can't issue an odd address to PCI area.

If Coral is the master device and the beginning address is set to the odd address in 64-bit boundary, Coral issue the previous even address.

Note: The odd address in 64 bit boundary means 0x04, 0xC.

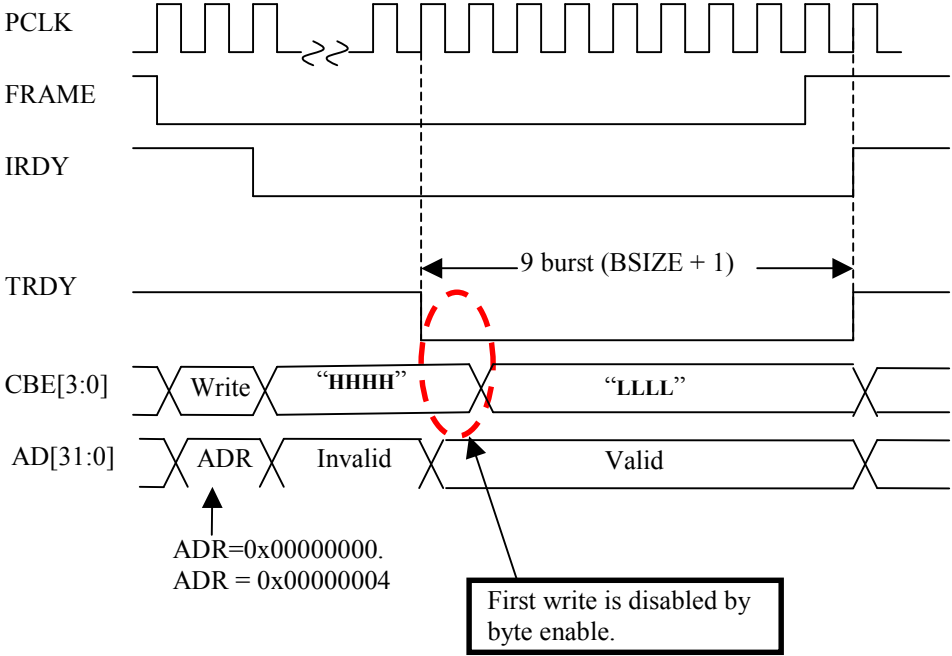
In Coral master read mode, Coral begins to read the previous even address and read the setting of burst size(BSIZE of BCR) plus "1".

Ex. Source address=0x00000004, BSIZE of BCR = 8,



In **Coral master write mode**, Coral begins to write the previous even address with disable write byte enable and write the setting of burst size(BSIZE of BCR) plus "1".

Ex. Source address=0x00000004, BSIZE of BCR = 8,



15-2. Coral = PCI Slave.

Phenomenon:

Coral reply the wrong data, if the read burst size comes more than the setting of SRBS.

This phenomenon occurs only burst read.

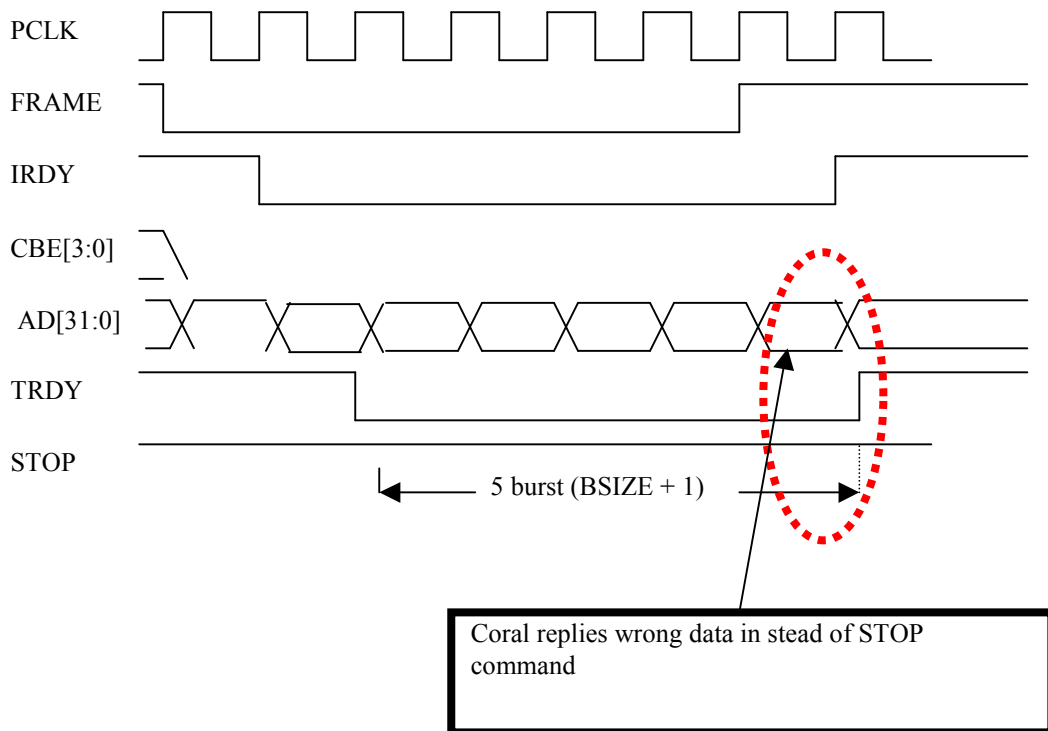
In burst write, Coral is able to issue the STOP command if there is no more available internal buffer.

Detail:

Coral replies the retry until storing the SRBS size data to Coral's PCI internal buffer.

After stored the data, Coral begins to reply the data by TRDY. But if the burst read comes more than the size of SBRBS, Coral replies the wrong data instead of issuing the STOP.

Ex. BSIZE of BCR = 4, Master issues the **burst read** more than "BSIZE+1" from Coral.



The Coral can fail in case of multi master access and a local DMA are running at the same time.

(a) Conditions:

- (1) Two PCI masters access Coral-PA via PCI bus. One master (Master-A) writes data to the memory which connected to Coral-PA. Another master (Master-B) reads data from the Coral-PA. These two transactions are executed independently and simultaneously. The problem does not occur, if both master are reading or writing to the Coral.
- (2) The "Local Display List" transfer and rendering operation are initiated at the same time.

(b) phenomenon

Because of the two independent data transfer from PCI master-A and B, it happens that write transaction from master-A occurs just after RETRY response of PCI from Coral-PA for the preceding read transaction of master-B. In certain condition of internal timing of Coral-PA among above transaction occurring, the write transaction by Master-A fails as the phenomenon that the data is written to different address intended (wrong address is used for the write transaction). In this problem, the wrong address value was swapped from the series of the data originally intended to store the memory. Therefore, the value of the wrong address is random value in general.

This problem occurs only in case the "Local Display List" transfer is initiated at the same time.

(b) workaround:

The access to the Coral must be synchronised.

Local DMA and multi master access may not occur at the same time. A single master access during a local DMA is running does not evoke the problem.

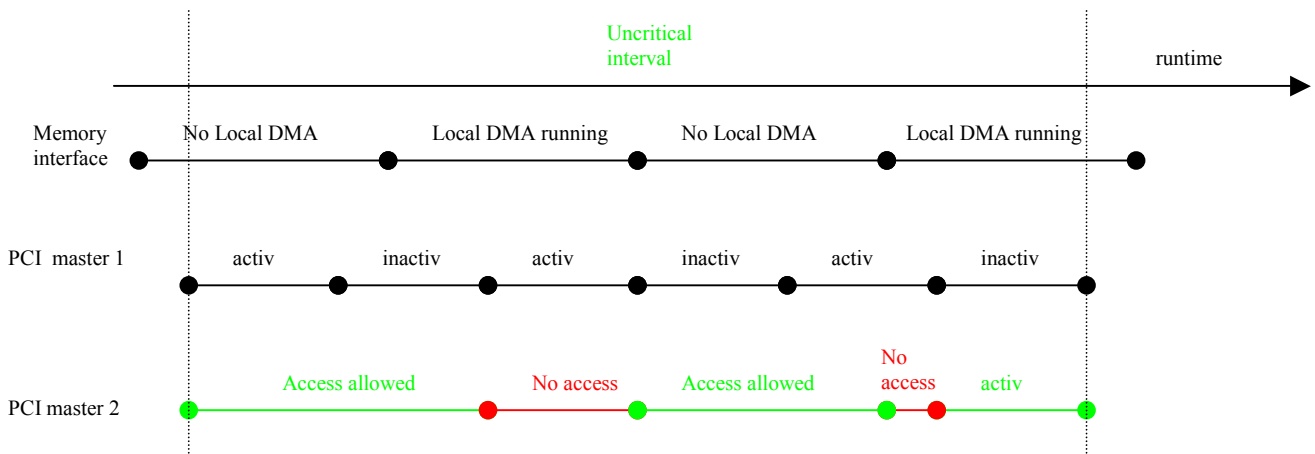


Figure 1 synchronising the access to the Coral

E12:
Video layer is not displayed

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conditions:

up-scaling is enabled

phenomenon:

The synchronisation between video capturing and display controller can fail.

The video layer data are not transmitted to the video output and the video layer is not visible on the display.

workaround:

The phenomenon does not occur, if the following sequence is kept for enabling the video input:

- 1) Set L1WY=0x0ffe and VSFC=0x07ff. (VSFC is in CSC register)
- 2) Set VIE=1 to start capture. (VIE is in VCM register)
- 3) Wait VSYNC two times
- 4) Set L1WY and VSFC with preferable values for application, respectively.