

# Errata Sheet MB86292 Orchid

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## History

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E1:  
DMA Transfer to FIFO

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#### **Details**

The DMA transferring to FIFO of Cremson has following regulations.

#### **CPU type:SH4/V83x**

Add an interrupt command(0xFD000000) at the end displaylist.

CPU prohibits to access to registers and memory of Cremson at the beginning of DMA transferring until occurring a interrupt of Cremson,

And "Dual DMA Transferring with 32Byte mode" at SH4 prohibits..

In case of "single DMA Transferring" at SH4, before executing this transfer, you have to set 0x00000001 to "Hostbase + 0x001c".

#### **CPU type:SH3**

Prohibit to use DMA transfer.

If you don't apply for these regulations, a long wait(some msec order) would be occurred by XRDY signal of Cremson. Then system memory on CPU bus could not be refreshed and a system would be unstable.

This regulations apply for "transferring to FIFO".

In case of "transferring to Graphics memory", you don't need to apply these regulations..

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E2:  
Read CTR register during local transferring

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#### **Details**

During local transferring, if CPU tries to read CTR register, a long wait would be occurred by XRDY.

#### **Measure**

Before starting local transferring, please set 0x00000001 to "Hostbase + 0x001c"

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E3:  
Differences of texture

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#### **Details**

In case the triangle with texture is drawn using Z coordinates or alpha / logical operation, ST coordinates may shift and the texture pattern may blur.

#### **Cause**

When Wait is generated at Z-buffer READ or frame buffer READ, the divider for texture perspectives continues moving while some of main pipeline was stopped. It cases this bug.

#### **measure**

There is no perfect avoidable measure. The blur of texture pattern becomes inconspicuous by using bi-linear filtering

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E4:  
Add initialize routine

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### Details

Before issue a displaylist, please execute these write.

Please write following "Data" to following "0x1ff8000 + offset".

Offset	Data
0x3fec	: 0x1ae7
0x3fe8	: 0x3ef2
0x3fe4	: 0x1ae9
0x3fe0	: 0xdb03
0x3fdc	: 0x1aea
0x3fd8	: 0xb612
0x3fd4	: 0x1aeb
0x3fd0	: 0xb612
0x3fcc	: 0x0001

Please write following "Data" to following "0x1ff8000 + offset".

Offset	Data
0x3fec	: 0x007e
0x3fe8	: 0xbf00
0x3fe4	: 0x007f
0x3fe0	: 0x1410
0x3fdc	: 0x00fe
0x3fd8	: 0xbf00
0x3fd4	: 0x00ff
0x3fd0	: 0x1422
0x3fcc	: 0x0001

If you use Graphics Driver that made by Fujitsu, you don't need above writings.  
GdcGeolInitialize( GDC\_TYPE\_MB86292 ) command does above writings.

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E5:  
Accessing the I2C interface registers(MB86292S only)

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### Detail

If CPU tries to read or write the I2C registers during the local transfer, the GDC does NOT reply XRDY signal. This means the system is hung-up.

The phenomenon does NOT occur during the DMA transfer.

### Measure

Don't read or write I2C registers during the local transfer.

Check the transfer status by bit 0 of LSTA(HostBase+0010) before read or write I2C registers.