

MB86291A "Scarlet A-version" Errata Sheet

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Additional SID Register in MB86291A
This register should be set to 0x03 by the user to prevent the "long wait" effect.
This register also indicates the version of Scarlet (non-A or A version). In the non-A version, the version-bits of this register are read as "0", in the A-version, this register returns "1".

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Other software or hardware bugs which have not been fixed.

Overview

This Errata-Sheet provides information on the MB86291A "Scarlet A-version" hardware changes.

The list for MB86291 revision

ID	Title	Description	Action
1	The bug of geometry firm	The case of view port tranformation of the coordinate before geometry clip generating is carried out or the case of not fitting [-4096,4095], the arbitrary polygon may not be drawn correctly. Because the circumscribed quadrangle is not renew correctly, illegal flag clear is genelated for un intended memory space. Therefore it is cause destroy of memory and performance degradation. It also may not be drawn correctry when W clip is generated, because there are the case of view port tranformation of the coordinate before W clip generating is carried out or the case of not fitting [-4096,4095].	At the peak where renewal of circumscription quadrangle protrudes geometry clip frame, firm revision is carried out so that it may not be carried out.
2	The bug about drawing omission of DrawRectP DrawBitmapP command	When rendering command of {DrawRectP, DrawBitmapP} is executed immediatly after a triangle, a straight line and a point are drawn by Scarlet rendering command, drawing of a few word of starting part of {DrawRectP,DrawBitmapP} may not be carried out.	It corrects so that a drawing change may be performed appropriately.
3	The bug 1 about CTR register read	If CTR register is read at the time of local transmission, long wait may occur.	Control which wait is not applied to CTR read in the case of long wait is performed (at time of FIFO full of local transfer). conventionally operation and a mode change are possible.
4	The bug 2 about CTR register read	Long wait may occur in GCTR register read after GCTR register write at the time of geometry FIFO use.	The negate timing of DREQ is corrected so that FIFO may carry out in the state of nearfull. conventionally operation and a mode change are possible.
5	The bug about DREQ negate timing	DREQ negate may be released when sampling time of DREQ is performed after read cycle. Demand transfer mode is applicable.	It is possible to avoid this bug as a result by coping with ID 4.
6	The long wait at the time of IST register read and write	When set to FIFO full in primitive drawing of long drawing time, long wait may occur in IST register access. Moreover, long wait may occur in IST register read after write to host interface register.	It is possible to avoid this bug as a result by coping with ID 4.
7	The long wait at the time of graphics memory access with a built-in GDC	If built-in graphics memory is accessed in primitive drawing of long drawing time, long wait may occur.	It is possible to avoid this bug as a result by coping with ID 4.
8	The long wait at the time of GDC display related register access	If display related register is accessed in pimitive drawing of long drawing time, long wait may occur.	It is possible to avoid this bug as a result by coping with ID 4.
9	The action of texture omission	Since priority is given to host interface access when access of drawing engine and host interface competes for the built-in texture memory, texture pattern may fall out in texture triangle drawing. For example, the phenomenon is checked when AC spec of host interface signal is not filled.	It corrects so that the mask of illegal access like the following can be carried out by adding decode condition of chip select signal inside of Scarlet.
10	Addition of chip version register	If there is a register which shows chip version which can distinguish the present Scarlet and the revision version, it will become easy to carry out version management from the software side.	The register which shows a chip version is added.

[MB86291A additional register]

SID(Scarlet ID)

Register Address	HostBaseAddress + 003ch																															
Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field name	ID																												Reserved		LW	DCF
R/W	R																												R0		RW	RW
Initial value	0001																												0		0	0

This register is added in MB86291A. This register is used for the additional mode regarding long wait of host I/F and the version indicator of MB86291 series. In MB86291, this register is reserved and the return value is zero.

- Bit0 DCF (DMA/CPU-write FIFO full control mode)
 This mode bit is used for FIFO full behavior control in case of DMA transfer or CPU-write
 0: FIFO full means when the stack data number in FIFO is 32. (The same as MB86291)
 1: FIFO full means when the stack data number in FIFO is 16.
- Bit1 LW (Local DMA Wait mode)
 This mode bit is used for the wait behavior control of local display list transfer. It can control the wait of CTR/GCTR-read from host CPU under FIFO full.
 0: In case of local display list transfer, MB86291A wait the termination of CTR/GCTR-read transaction when CTR/GCTR-read occurred under FIFO full. (The same as MB86291)
 1: In case of local display list transfer, MB86291A does not wait the termination of CTR/GCTR-read transaction when CTR/GCTR-read occurred under FIFO full.
- Bit27-2 Reserved
- Bit31-28 SID(Scarlet ID)
 This mode bit indicates ID of MB86291 series.
 0: MB86291
 1: MB86291A

APPENDIX 1 [BLPO register]

1. details of the bug

Because of a bug in write function of BLPO (Broken Line Pattern Offset) register which is described in Specification [10.1.6 draw mode register], an arbitrary value cannot be set to BLPO register.

2. cause of the bug

It is the cause that BLPO register is overwritten with the value of BLPO mirror register which has internally the value which was written to BLPO register.

3. measure

It is in the following cases that the bug causes a problem.

A: A broken line is used.

B: Another primitive is drawn. Or a not continuous broken line is used.

C: A continuation of the broken line of A is drawn so that it may be continued to the line of A.

In this case, an arbitrary value has to be applied to BLPO register at process of C. But this cannot be performed because of this bug.

There is the following method as an avoidable measure to the bug.

Please change the broken line pattern.

For example, when you want to draw the following the broken line pattern(direction: from left to right) again,

□□■■■■□□□■□□□■□□■■■...



When you want to continue drawing from here.

Please change the broken line pattern to ■□□□■□□■■■

Then clear the broken line pointer and start drawing.

4. correction of hardware

This bug will be corrected at the time of the following revision.

APPENDIX 2 [differences of texture]

1. details of the bug

In case the triangle with texture is drawn using Z coordinates or alpha / logical operation, ST coordinates may shift and the texture pattern may blur.

2. cause of the bug

When wait is generated at Z-buffer READ or frame buffer READ, the divider for texture perspectives continues moving while some of main pipeline was stopped. This causes this bug.

3. measure

There is no perfect avoidable measure. The blur of texture pattern becomes inconspicuous by using bi-linear filtering.

4. correction of hardware

no hardware correction is planned for this bug.