

Errata Sheet MB86290A Cremson

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History

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E1:
DMA Transfer to FIFO

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Details

The DMA transferring to FIFO of Cremson has following regulations.

CPU type:SH4/V83x

Add an interrupt command(0xFD000000) at the end displaylist.
CPU prohibits to access to registers and memory of Cremson at the beginning of DMA transferring until occurring a interrupt of Cremson,
And "Dual DMA Transferring with 32Byte mode" at SH4 prohibits..
In case of "single DMA Transferring" at SH4, before executing this transfer, you have to set 0x00000001 to "Hostbase + 0x001c".

CPU type:SH3

Prohibit to use DMA transfer.

If you don't apply for these regulations, a long wait(some msec order) would be occurred by XRDY signal of Cremson. Then system memory on CPU bus could not be refreshed and a system would be unstable.

This regulations apply for "transferring to FIFO".

In case of "transferring to Graphics memory", you don't need to apply these regulations..

E2:
Read CTR register during local transferring

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Details

During local transferring, if CPU tries to read CTR register, a long wait would be occurred by XRDY.

Measure

Before starting local transferring, please set 0x00000001 to "Hostbase + 0x001c"

E3:
Pattern (Text) Drawing

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Details

Pattern (Text) Drawing does not work correctly in case of character pattern enlarged 2x2, x2 horizontal at 16 bit color mode.

Conditions

Pattern drawing with 2x2 or x2 horizontal at 16 bit color mode.
Drawing starting point is second pixel from 32 bit align.

Example

Bitmap pattern:0x000000d

x2 horizontal

:Fore Color ●

:Back Color ○

The expectation : ●●○○●●●●○○

The fact : ●●○○●○○●●●○○



This pixel is drawn by bit1 data.

Measure

Don't use this command with enlarging 2x2 or x2 horizontal at 16 bit color mode.

Make a binary pattern to be same bit1 and bit2.

.At first draw at 32 bit align area, then copy it to a point where you want to draw.

E4:
BltCopy with logical calculation

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Details

When you draw BltCopy command with logical calculation, a vertical line of draw starting point doesn't draw correctly. This will be occurred both 16 bit color mode and 8 bit color mode. BltCopyAlternate command doesn't occur this problem. The logical calculation type occurred this problem is follows.

-In case of copying to another point.

AND REVERSE
XOR
NOR
EQUIV
INVERT
OR REVERSE
NAND

-In case of copying to same point.

(Copying to same point is for draw black by copying with XOR.)

NOR
INVERT
COPY INVERT
NAND

Measure

At first, copy a original data to somewhere, then copy it from there using BltCopyAlternateP command with logical calculation.

E5:
BltCopy for moving data to only vertical direction.


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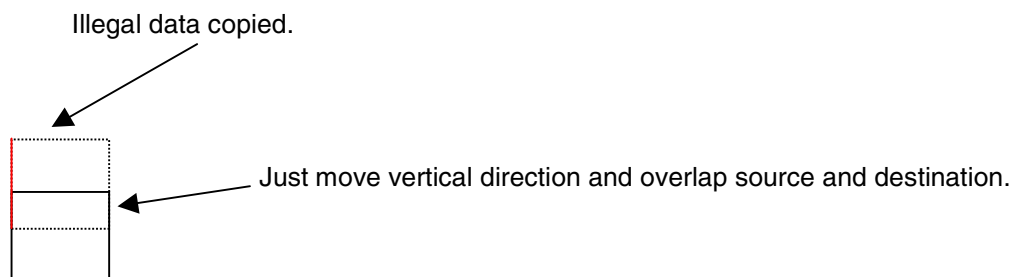
Details

When you use Bltcopy for just moving to vertical direction and overlap source data area and destination area, a source data is broken.

Example

Command: BltCopy

 : Source data
: Destination area



In this case, a command uses TopLeft.
The 1 pixel red line data is wrong.

In case of xxxLeft command, Left side of 1 pixel line changes wrong data.
In case of xxxRight command, Right side of 1 pixel line changes wrong data.

Measure

Make work area somewhere, at first copy data there, then copy it destination.

E6:

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Memory that is possible to connect with Cremson.

Details

Cremson accepts a memory that "write recovery time" is only 1 clock.

"write recovery time" is the time that data-in command to read or pre-charge time.

Some memory requests 2 clocks.

Memory which is possible to connect.

Manufacture	Parts name
Hitachi	HM5264165F 64Mbit x16 SDRAM
NEC	uPD4564323 64Mbit x32 SDRAM
Toshiba	TC5956432CFT 64Mbit x32 SDRAM
Hyundai	HY57V651620BTC-10 64Mbit x32 DSRAM
MICRON	MT48LC2M32B2 64Mbit x32 SDRAM

Impossible to connect

SAMSUNG,
Infineon

E7:

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About Specification sheet of MB86290A

a) WOA register

About W layer, there is WOA register and WDA register in specification sheet.

But W layer can't do rap around function, so WDA register is only available.

b) Pin Assignment Diagram

There is wrong descriptions about "2.2.1.Pin Assignment Diagram" at 21 page of Specification Sheet.

The discription of "2.2.2 Pin Assignment Table" at 22 page are correct.

Pin No	Wrong	Correct
212	: AVS1	-> ACOMPB
213	: AOUTB	-> AVD1
214	: AVD1	-> AOUTB
215	: ACOMPB	-> AVS1
222	: ACOMPR	-> AVS4
223	: VREF	-> AOUTR
224	: VRO	-> AVD4
225	: AVD4	-> VRO
226	: AOUTR	-> VREF
227	: AVS4	-> ACOMPR