

## ASSP for Graphics Control

# Graphics Display Controller

## MB86290A

### ■ DESCRIPTION

The MB86290A is a graphics display controller for drawing and displaying graphics on a car navigation system or amusement unit.

The MB86290A can process high-quality, true three-dimensional graphics at high speed using advanced features such as distortion control and hidden surface removal during expression of various levels of transparency and drawing in three-dimensional space. It can also process two-dimensional graphics with a smooth touch, for example, by drawing smooth lines and drawing polygons by connecting arbitrarily specified vertices.

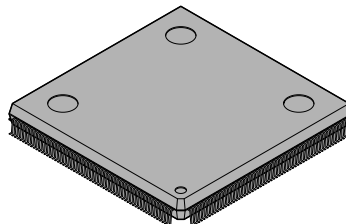
### ■ FEATURES

- Operating frequency: 100 MHz (External clock of 14.32 MHz Max)
- Host interface: Enables direct connection to a CPU (Hitachi SH3/4 or NEC V832).
- Drawing features:
  - Drawing at a peak rate of 800 Mpixels per second (at an internal operating frequency of 100 MHz)
  - 2D drawing functions: Point, line, triangle, polygon, BLT, and pattern drawing
  - 3D drawing functions: Point, line, and triangle drawing, and hidden surface removal by Z-buffering
  - Special effects: Anti-aliasing, bold/dashed-line processing, alpha blending, Gouraud shading, texture mapping (bilinear filtering, perspective correct), and tiling

(Continued)

### ■ PACKAGE

240-pin, Plastic QFP



(FPT-240P-M03)

# MB86290A

*(Continued)*

- Display features :
  - Maximum display resolution supported: 1024 x 768 pixels
  - Color display either with a color palette of 8 bits per pixel or directly using 5-bit RGB colors of 16 bits per pixel
  - Overlaying four layers of screen, of which two lower layers can be divided into the left and right parts
  - Supporting two 64x64-pixel hardware cursors
  - Three-channel D/A converter integrated to output analog RGB signals
  - Capable of superimposing using an external synchronization mode
- Memory interface :
  - Using SDRAM as graphics memory at an operating clock speed of 100 MHz and data bus width of 64 bits. Capable of connecting up to 32 Mbytes (offering a throughput of 800 Mbps).
  - Power-supply voltage: Two power supplies at 2.5 V $\pm$ 0.2 V for internal circuits and 3.3 V $\pm$ 0.3 V for I/O parts
  - Package: Plastic QFP with 240 pins (with a lead pitch of 0.5 mm)
  - Power consumption: 1 W (at 100 MHz, V<sub>DDL</sub> = 2.5 V  $\pm$  0.2 V)
  - Process technology: 0.25  $\mu$ m CMOS

## PIN ASSIGNMENT

(TOP VIEW)

INT	1	240	TEST4	180	WE3
DR	2	239	MODE1	179	WE2
RDY	3	238	MODE0	178	WE1
D0	4	237	DCLKI	177	WE0
D1	5	236	VDDL	176	DTACK/TC
D2	6	235	VSS	175	DRACK/DMAAK
D3	7	234	VDDH	174	RD
D4	8	233	DCLKO	173	CS
D5	9	232	HSYNC	172	VDDL
D6	10	231	VSNC	171	VSS
D7	11	230	CSYNC	170	BCLKI
D8	12	229	GV	169	BS
D9	13	228	EO	168	TEST2
VDDH	14	227	ACOMPR	167	TEST1
VSS	15	226	VREF	166	TEST0
VDDL	16	225	VRO	165	AVS0
D10	17	224	AVD4	164	S
D11	18	223	AOUTR	163	CLK
D12	19	222	AVS4	162	AVD0(VCO)
D13	20	221	AVS3	161	RESET
D14	21	220	AVD3	160	VDDL
D15	22	219	AVS2	159	VSS
D16	23	218	AOUTG	158	MD63
D17	24	217	AVD2	157	MD62
D18	25	216	ACOMP	156	MD61
D19	26	215	AVS1	155	MD60
D20	27	214	AOUTB	154	MD59
D21	28	213	AVD1	153	MD58
D22	29	212	ACOMP	152	MD57
VDDH	30	211	<OPEN>	151	VSS
VSS	31	210	TEST3	150	VDDH
VDDL	32	209	CKM	149	MD56
D23	33	208	A24	148	MD55
D24	34	207	VSS	147	MD54
D25	35	206	A23	146	MD53
D26	36	205	A22	145	MD52
D27	37	204	A21	144	MD51
D28	38	203	A20	143	MD50
D29	39	202	A19	142	VSS
D30	40	201	A18	141	MD49
D31	41	200	VDDL	140	MD48
VSS	42	199	VSS	139	MD47
MD0	43	198	A17	138	MD46
MD1	44	197	A16	137	MD45
MD2	45	196	A15	136	MD44
MD3	46	195	A14	135	MD43
VDDH	47	194	A13	134	MD42
VSS	48	193	A12	133	VDDL
VDDL	49	192	A11	132	VSS
MD4	50	191	A10	131	VDDH
MD5	51	190	A9	130	MD41
MD6	52	189	A8	129	MD40
MD7	53	188	VDDL	128	MD39
MD8	54	187	VSS	127	MD38
MD9	55	186	A7	126	MD37
MD10	56	185	A6	125	MD36
MD11	57	184	A5	124	MD35
MD12	58	183	A4	123	MD34
MD13	59	182	A3	122	MD33
	60	181	A2	121	MD32
MD14	61				
MD15	62				
MD16	63				
MD17	64				
VDDH	65				
VSS	66				
VDDL	67				
MD18	68				
MD19	69				
MD20	70				
MD21	71				
MD22	72				
MD23	73				
MD24	74				
VSS	75				
MD25	76				
MD26	77				
MD27	78				
MD28	79				
MD29	80				
MD30	81				
MD31	82				
VDDH	83				
VSS	84				
VDDL	85				
MDQM0	86				
MDQM1	87				
MDQM2	88				
MDQM3	89				
MRA5	90				
MCA5	91				
MVE	92				
MA0	93				
MA1	94				
MA2	95				
MA3	96				
MA4	97				
VDDH	98				
VSS	99				
MA5	100				
MA6	101				
MA7	102				
MA8	103				
MA9	104				
MA10	105				
MA11	106				
MA12	107				
MA13	108				
CKE	109				
MCLKO	110				
VDDH	111				
VSS	112				
VDDL	113				
MCLKI	114				
TEST5	115				
VSS	116				
VSS	119				
MDQM4	117				
MDQM5	118				
MDQM6	119				
MDQM7	120				

VSS/AVS : Ground, VDDH : 3.3 V power supply, VDDL : 2.5 V power supply

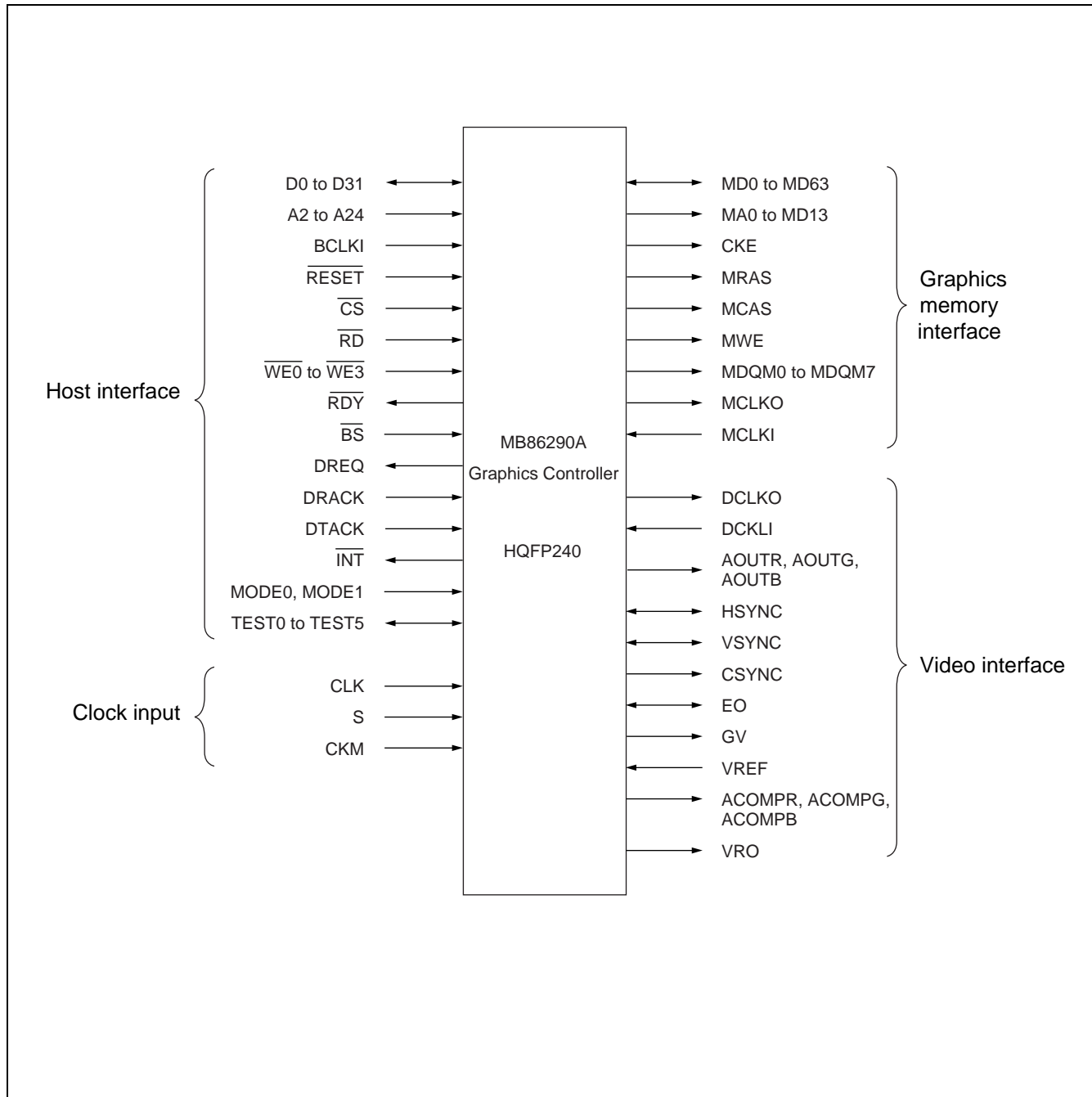
AVD1 - AVD4 : 2.5 V analog power supply, AVD(VCO) : 2.5 V PLL power supply

Notes : • Leave pin 211 open without making any connection.

• AVD1 - AVD4, AVD(VCO), and /VDDL should be separated on the board.

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## ■ PIN DESCRIPTION



## • Host Interface Pins

Pin Name	Input/output	Function
MODE0, MODE1	Input	Host CPU mode select
$\overline{\text{RESET}}$	Input	Hardware reset
D0 to D31	Input/Output	Host CPU bus data
A2 to A24	Input	Host CPU bus address (Connect A24 to $\overline{\text{MWR}}$ in V832 mode.)
BCLKI	Input	Host CPU bus clock
$\overline{\text{BS}}$	Input	Bus cycle start signal
$\overline{\text{CS}}$	Input	Chip select signal
$\overline{\text{RD}}$	Input	Read strobe signal
$\overline{\text{WE0}}$	Input	D0 to D7 write strobe signal
$\overline{\text{WE1}}$	Input	D8 to D15 write strobe signal
$\overline{\text{WE2}}$	Input	D16 to D23 write strobe signal
$\overline{\text{WE3}}$	Input	D24 to D31 write strobe signal
$\overline{\text{RDY}}$	Output Tristate	Wait request signal ("0" for wait state with SH3; "1" for wait state with SH4 or V832)
DREQ	Output	DMA request signal (active low with both SH and V832)
DRACK/ DMAAK	Input	InputDMA request acknowledge signal (Connect this to DMAAK in V832 mode. Active high with both SH and V832.)
DTACK/ $\overline{\text{TC}}$	Input	DMA transfer strobe signal (Connect this to $\overline{\text{TC}}$ in V832 mode. SH = active high, V832 = active low)
$\overline{\text{INT}}$	Output	Host CPU interrupt signal (SH = active low, V832 = active high)
TEST0 to TEST5	Input	Test signal

Note : The host interface can connect the MB86290A to the SH4 (SH7750) or SH3 (SH7709) manufactured by Hitachi Ltd. or to the V832 manufactured by NEC without any external circuit in between. (Using the SRAM interface allows the MB86290A to use another CPU.) The host CPU is set by the MODE pins as shown below.

MODE1 pin	MODE0 pin	CPU Type
L	L	SH3
L	H	SH4
H	L	V832
H	H	Reserved

- Notes :
- The host interface transfers data signals at a fixed width of 32 bits.
  - There are 23 lines for address signals handled in double words (32 bits) and 32 Mbytes of address space.
  - The external bus can be used at an operating frequency of 100 MHz Max.
  - The  $\overline{\text{RDY}}$  signal at the low level sets the ready state in the SH4 or V832 mode; the signal at the low level sets the wait state in the SH3 mode. Note that the  $\overline{\text{XRDY}}$  signal is a tristate output.
  - The host interface supports DMA transfer using an external DMA controller.

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- The host interface generates a host processor interrupt signal.
- The RESET pin requires low level input of at least 300  $\mu$ s after setting "S" (PLL reset signal) to high level.
- Fix the TEST signal at high level.
- In the V832 mode, connect the following pins as specified :

Pin Name	V832 Signal Name
A24	$\overline{MWR}$
DTACK	$\overline{TC}$
DRACK	DMAAK

## • Video Interface Pins

Pin Name	Input/output	Function
DCLKO	Output	Display dot clock signal output
DCLKI	Input	External synchronous dot clock signal input
AOUTR	Analog output	Analog video (R) signal output
AOUTG	Analog output	Analog video (G) signal output
AOUTB	Analog output	Analog video (B) signal output
HSYNC	Input/output*	Horizontal sync signal output Horizontal sync signal input in external synchronization mode
VSYNC	Input/output*	Vertical sync signal output Vertical sync signal input in external synchronization mode
CSYNC	Output	Composite sync signal output
EO	Input/output*	Even/odd-number field identification output Even/odd-number field identification input in external synchronization mode
GV	Output	Graphics/video select signal
VREF	Analog output	Reference voltage input pin
ACOMPR	Analog output	R-signal compensation pin
ACOMPG	Analog output	G-signal compensation pin
ACOMPB	Analog output	B-signal compensation pin
VRO	Analog output	Reference current setting pin

\* : Input voltage level : 5 V tolerant

- Notes :
- The video interface contains an 8-bit D/A converter to output analog RGB signals.
  - Using an additional external circuit, the video interface can use CSYNC signals to generate composite video signals.
  - The video interface can output analog RGB signals synchronized with external video signals. The mode for synchronization with the DCLKI signal can be selected as well as the mode for synchronization with a set dot clock as for normal display.
  - The HSYNC and VSYNC signals must be pulled up outside the LSI as they enter the input state upon reset.
  - Terminate the AOUTR, AOUTG, and AOUTB pins with a resistance of 75  $\Omega$ .
  - Input 1.1 V to the VREF pin. Between this pin and analog ground, insert a bypass capacitor (one with a superior high-frequency characteristic such as a laminated ceramic capacitor) .
  - Connect the ACOMPR, ACOMPG, and ACOMPB pins to the 0.1  $\mu$ F ceramic capacitor ahead of the analog power supply.
  - Connect the VRO pin to the analog ground with a 2.7 k $\Omega$  resistor.
  - The input voltage levels of the HSYNC, VSYNC, and EO signals are 5 V tolerant. Do not input 5 V to these pins with the power supply off. (See ■ ABSOLUTE MAXIMUM RATINGS.)
  - For noninterlaced display in external synchronization mode, input "0" to the EO pin, for example, using a pull-down resistor.
  - The GV signal serves to switch between graphics and video for chroma keying. The pin outputs a low level signal to select video.

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## • Graphics Memory Interface Pins

Pin Name	Input/output	Function
MD0 to MD63	Input/output	Graphics memory bus data
MA0 to MA13	Output	Graphics memory bus data
CKE	Output	Clock enable
MRAS	Output	Row address strobe
MCAS	Output	Column address strobe
MWE	Output	Write enable
MDQM0 to MDQM7	Output	Data mask
MCLKO	Output	Graphics memory clock output
MCLKI	Input	Graphics memory clock input

- Notes :
- The graphics memory interface connects the MB86290A to the external memory used for graphical image data. The interface can directly accept 64 Mbit SDRAM (with a 16-bit or 32-bit data bus) without any external circuit.
  - The data signal can be selected between 64 bits and 32 bits. To use the 32-bit signal, leave the MD32 to MD63 and MDQM4 to MDQM7 pins open.
  - Connect the MCLKI pin to the MCLKO pin.

## • Clock Input Pins

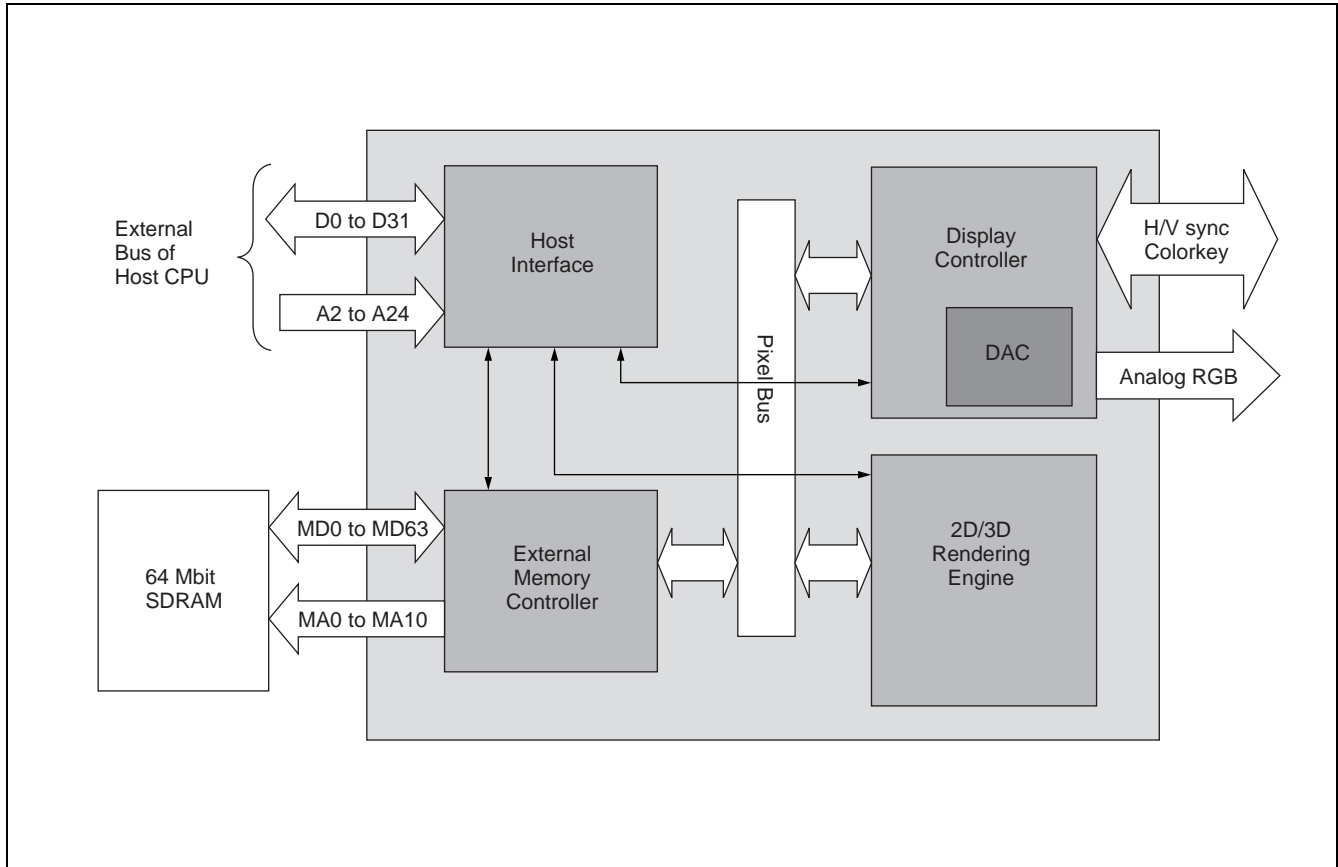
Pin Name	Input/output	Function
CLK	Input	Clock input signal
S	Input	PLL reset signal
CKM	Input	Clock mode signal

- Notes :
- The clock input block inputs the clock signal that serves as the basis for the reference clock for the internal operating clock and display dot clock. Usually input 4 Fsc (= 14.31818 MHz). The internal PLL generates the internal operating clock signal of 100.22726 MHz and the display reference clock signal of 200.45452 MHz.
  - The internal operating clock signal to be used can be selected between the clock signal (CLK input multiplied by 7) generated by the internal PLL and the bus clock BCLKI input to the host CPU interface. Select the BCLKI input to use the host CPU bus at 100 MHz.

CKM	Clock Mode
L	Select internal PLL output.
H	Select host CPU bus clock (BCLKI) .

- Note : Immediately after turning the power supply on, input a pulse whose low level period is 500 ns or more to the S pin before setting it to high level. After the S signal goes high, input the  $\overline{\text{RESET}}$  signal at low level for 300  $\mu\text{s}$  or more.

## ■ BLOCK DIAGRAM



## ■ FUNCTION BLOCKS

- Host Interface

This block allows the MB86290A to be connected to the SH3 or SH4 microprocessor manufactured by Hitachi Ltd. without any external circuit in between. The block provides an interface to transfer display list and texture pattern data directly from main memory to the CREMSON graphics memory or internal register using the external DMA controller.

- External Memory Controller

This block controls the external synchronous DRAM connected as graphics memory. The 64-bit or 32-bit data bus is selected and the maximum operating frequency is 100 MHz.

- Display Controller

This block contains a three-channel D/A converter supporting XGA (1024x768 pixels) display and outputs analog RGB signals. The block enables superimposing using the external synchronization mode. It can divide the screen into the left and right parts to display different contents and to scroll them separately. It can also display animations smoothly using double buffering. In addition, it can overlay up to four screens, where the image color blending function can be used to display maps through the console screen as a transparency.

- 2D/3D Rendering Engine

This block draws images in two or three dimensions.

- 2D drawing

The block provides the anti-aliasing and alpha blending functions to display high-quality images even on a low-resolution LCD.

- 3D drawing

The block provides true 3D drawing functions such as perspective texture mapping and Gouraud shading.

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power-supply voltage	$V_{DDL}^{*1}$	- 0.5	+ 3.0	V
	$V_{DDH}$	- 0.5	+ 4.0	V
Input voltage	$V_I$		$V_{DDH} + 0.5 (< 4.0)$	V
	$V_{IV}^{*2}$	- 0.5	$V_{DDH} + 4.0 (< 6.0)$	
Output current	$I_O$	- 13	+ 13	mA
Power pin current	$I_{POW}$	—	60	mA
Ambient operating temperature	$T_A$	0	70	°C
		- 40 <sup>*3</sup>	+ 85 <sup>*3</sup>	
Ambient storage temperature	$T_{stg}$	- 55	+ 125	°C

\*1 : The analog and PLL power supplies are included.

\*2 : The HSYNC, VSYNC, and EO signals are input.

\*3 : Model supporting a wider range of temperatures

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power-supply voltage	$V_{DDL}^{*1}$	2.3	2.5	2.7	V
	$V_{DDL}^{*2}$	2.6 <sup>*6</sup>			
	$V_{DDH}$	3.0	3.3	3.6	
		3.5 <sup>*6</sup>			
Input voltage (High level)	$V_{IH}$	2.0	—	$V_{DDH} + 0.3$	V
	$V_{IHV}^{*3}$	2.0	—	5.5	
Input voltage (Low level)	$V_{IL}$	- 0.3	—	+ 0.8	V
	$V_{ILV}^{*3}$	- 0.3	—	+ 0.8	
VREF pin input voltage	$V_{REF}$	1.05	1.10	1.15	V
VRO pin external resistor	$R_{VRO}$	—	2.7	—	k $\Omega$
AOUT pin external resistor <sup>*4</sup>	$R_{AOUT}$	—	75	—	$\Omega$
ACOMP pin external capacitor <sup>*5</sup>	$C_{ACOMP}$	—	0.1	—	$\mu$ F
Ambient operating temperature	$T_A$	- 40	—	+ 85	$^{\circ}$ C
				+ 70 <sup>*6</sup>	

\*1 : The analog and PLL power supplies are included.

\*2 : The HSYNC, VSYNC, and EO signals are input.

\*3 : AOUTR, AOUTG, and AOUTB pins

\*4 : AOUTR, AOUTG, AOUTB pins

\*5 : ACOMPR, ACOMP G, ACOMP B pins

\*6 : Using BCLKI at 90 MHz or more

Notes : • The VDDL and VDDH power supplies can be turned on or off in either order.

Note, however, that the VDDH voltage must not be applied alone continuously for several seconds.

- Do not input the HSYNC, VSYNC or signal with the power-supply voltage not applied. (See “Input voltage” in “■ ABSOLUTE MAXIMUM RATINGS”.)
- After turning the power on, input a pulse remaining at low level for at least 500 ns to the S pin. Then, set the S pin to high level and input the  $\overline{RESET}$  signal held at low level for at least 300  $\mu$ s.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

( $V_{DDL} = 2.5 \text{ V} \pm 0.2 \text{ V}$ ,  $V_{DDH} = 3.3 \text{ V} \pm 0.3$ ,  $V_{SS} = 0.0 \text{ V}$ ,  $T_A = 0 \text{ }^\circ\text{C}$  to  $+70 \text{ }^\circ\text{C}$ )

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Output voltage (High level) *1		$V_{OH}$	$V_{DDH} - 0.2$	—	$V_{DDH}$	V
Output voltage (Low level) *2		$V_{OL}$	0.0	—	0.2	V
Output current (High level)		$I_{OH1}$ *3	- 2.0	—	—	mA
		$I_{OH2}$ *4	- 4.0	—	—	
		$I_{OH3}$ *5	- 8.0	—	—	
Output current (Low level)		$I_{OL1}$ *3	2.0	—	—	mA
		$I_{OL2}$ *4	4.0	—	—	
		$I_{OL3}$ *5	8.0	—	—	
AOUT voltage*6	Full scale	$I_{AOUT}$	9.90	10.42	10.94	mA
	Zero scale		0	2	20	$\mu\text{A}$
AOUT voltage*7		$V_{AOUT}$	- 0.1	—	+ 1.1	V
Input leakage current		$I_L$	—	—	$\pm 5$	$\mu\text{A}$
Pin capacitance		C	—	—	16	pF

\*1 : Value when  $-100 \mu\text{A}$  current flows into output pins.

\*2 : Value when  $100 \mu\text{A}$  current flows into output pins.

\*3 : Output characteristics of the MD0 to MD63, MDQM0 to MDQM7 pins

\*4 : Output characteristics of the signals (excluding analog signals) other than those in \*3 and \*5

\*5 : MCLKO pin output characteristics

\*6 : AOUTR, AOUTG, and AOUTB pin output current. Conditions  $V_{REF} = 1.10 \text{ V}$ ,  $R_{VRO} = 2.7 \text{ k}\Omega$   
(The full-scale output current calculation expression is  $(V_{REF} / R_{VRO}) \times 25.575$  )

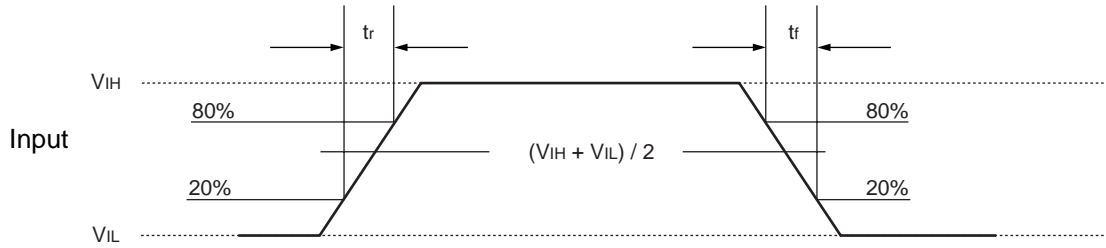
\*7 : AOUTR, AOUTG and AOUTB pins

# MB86290A

## 2. AC Characteristics

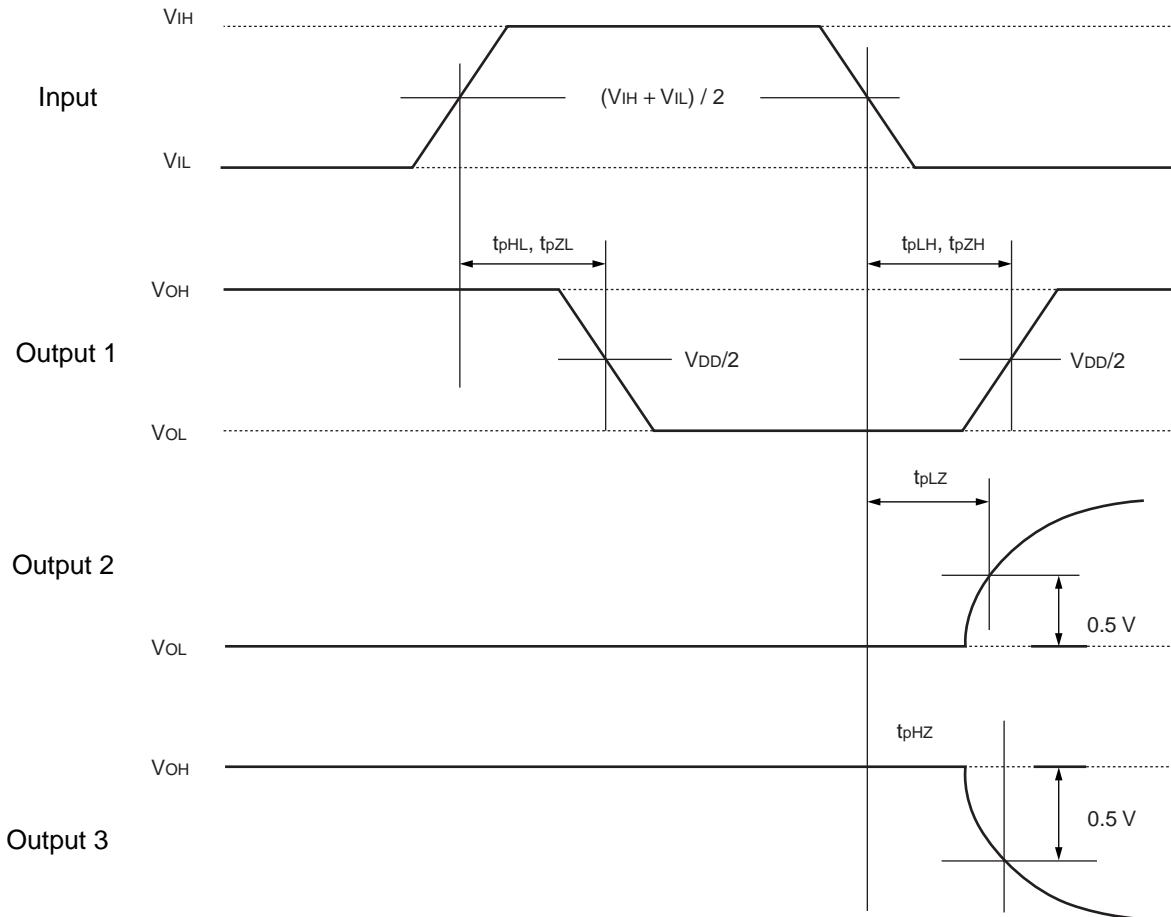
( $V_{IH} = 2.0\text{ V}$ ,  $V_{IL} = 0.8\text{ V}$ )

- Input measurement conditions



- $t_r, t_f \leq 5\text{ ns}$
- Input measurement standard :  $(V_{IH} + V_{IL}) / 2$

- Output measurement conditions



- Output measurement standard :  $t_{pLZ} : V_{OL} + 0.5\text{ V}$   
 $t_{pHZ} : V_{OH} - 0.5\text{ V}$   
 Else :  $V_{DD}/2$

## (1) Host Interface

### • Clock

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
BCLKI frequency	$f_{\text{BCLKI}}$	—	—	100	MHz
BCLKI H period	$t_{\text{HBCLKI}}$	—	3.5	—	ns
BCLKI L period	$t_{\text{LBCLKI}}$	—	3.5	—	ns

### • Host interface signals

(Recommended operating conditions A, External load of 20 pF)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Address setup time	$t_{\text{ADS}}$	—	3.0	—	ns
Address hold time	$t_{\text{ADH}}$	—	1.0	—	ns
$\overline{\text{BS}}$ setup time	$t_{\text{BSS}}$	—	3.5 3.0* <sup>3</sup>	—	ns
$\overline{\text{BS}}$ hold time	$t_{\text{BSH}}$	—	0.0	—	ns
$\overline{\text{CS}}$ setup time	$t_{\text{CSS}}$	—	3.5 3.0* <sup>3</sup>	—	ns
$\overline{\text{CS}}$ hold time	$t_{\text{CSH}}$	—	0.0	—	ns
$\overline{\text{RD}}$ setup time	$t_{\text{RDS}}$	—	3.0	—	ns
$\overline{\text{RD}}$ hold time	$t_{\text{RDH}}$	—	1.0	—	ns
$\overline{\text{WE}}$ setup time	$t_{\text{WES}}$	—	3.0	—	ns
$\overline{\text{WE}}$ hold time	$t_{\text{WEH}}$	—	1.0	—	ns
Write data setup time	$t_{\text{WDS}}$	—	5.0 4.0* <sup>3</sup>	—	ns
Write data hold time	$t_{\text{WDH}}$	—	1.0	—	ns
DTACK setup time	$t_{\text{DAKS}}$	—	3.0	—	ns
DTACK hold time	$t_{\text{DAKH}}$	—	1.0	—	ns
DRACK setup time	$t_{\text{DRKS}}$	—	3.0	—	ns
DRACK hold time	$t_{\text{DRKH}}$	—	1.0	—	ns
Read data delay time (to $\overline{\text{RD}}$ )	$t_{\text{RDDZ}}$	—	4.0	8.5	ns
			—	7.5* <sup>3</sup>	ns
Read data delay time	$t_{\text{RDD}}$	*1	4.0	9.5	ns
			—	6.0* <sup>3</sup>	ns
$\overline{\text{RDY}}$ delay time (to $\overline{\text{CS}}$ ) SH	$t_{\text{RDYDZ}}$	—	3.0	9.0	ns
			—	7.5* <sup>3</sup>	ns

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# MB86290A

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Parameter	Symbol	Condition	Value		Unit
			Min	Max	
$\overline{\text{RDY}}$ delay time (to $\overline{\text{CS}}$ ) V832	$t_{\text{RDYDZ}}$	—	3.0	13.0	ns
			—	10.5* <sup>3</sup>	ns
$\overline{\text{RDY}}$ delay time	$t_{\text{RDYD}}$	—	3.5	8.5	ns
			—	7.0* <sup>3</sup>	ns
DREQ delay time	$t_{\text{DRQD}}$	—	3.5	7.5	ns
			—	6.5* <sup>3</sup>	ns
MODE hold time	$t_{\text{MODH}}$	*2	—	20.0	ns

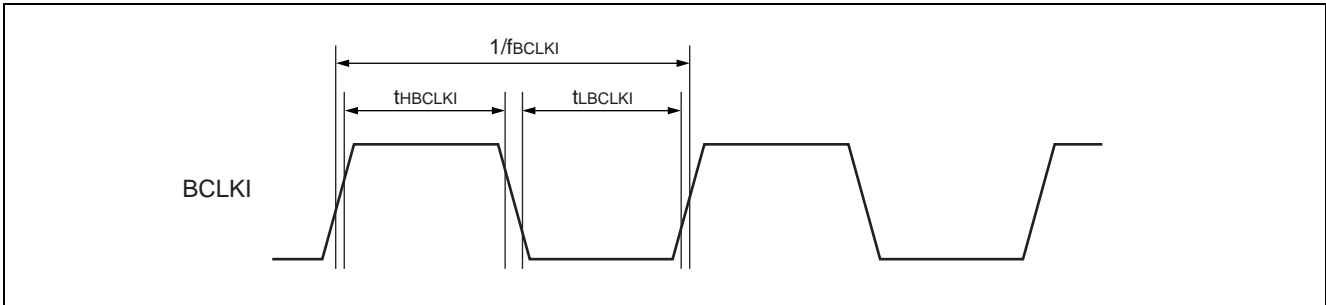
\*1 : Read data is output one cycle before the CPU samples it.

\*2 : Hold time for reset cancellation

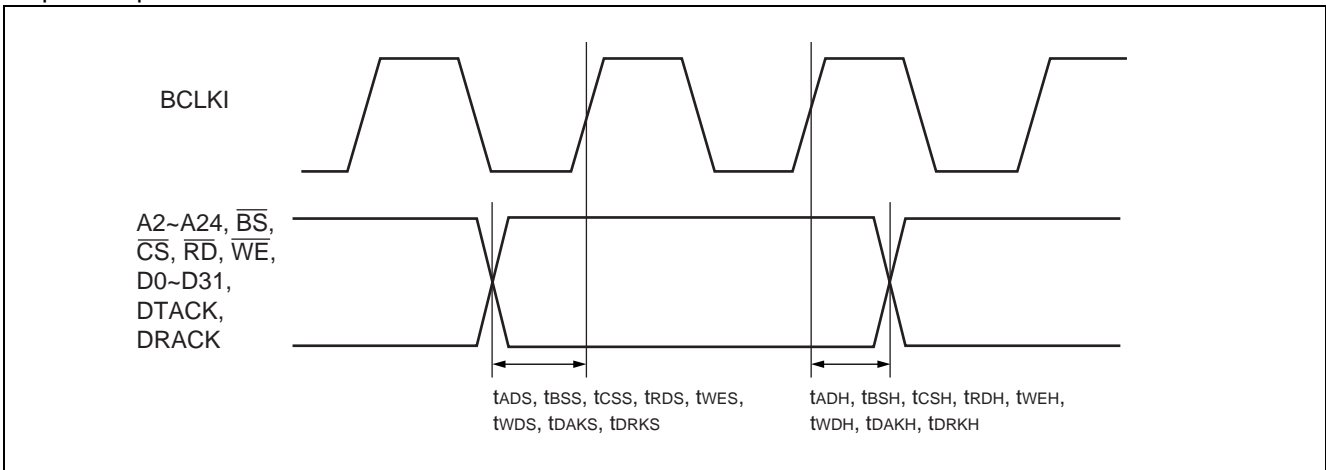
\*3 : Using BCLKI at 90 MHz or more

Note: The  $\overline{\text{INT}}$  signal is output in synchronization with the internal operating clock. As a host interface signal, it is an asynchronous signal.

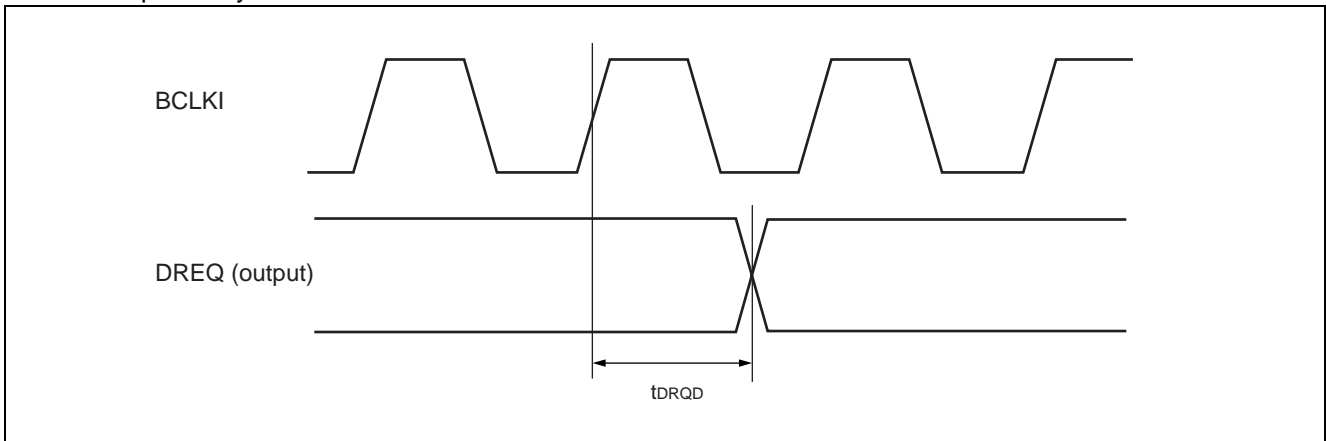
- Clock



- Input setup and hold times

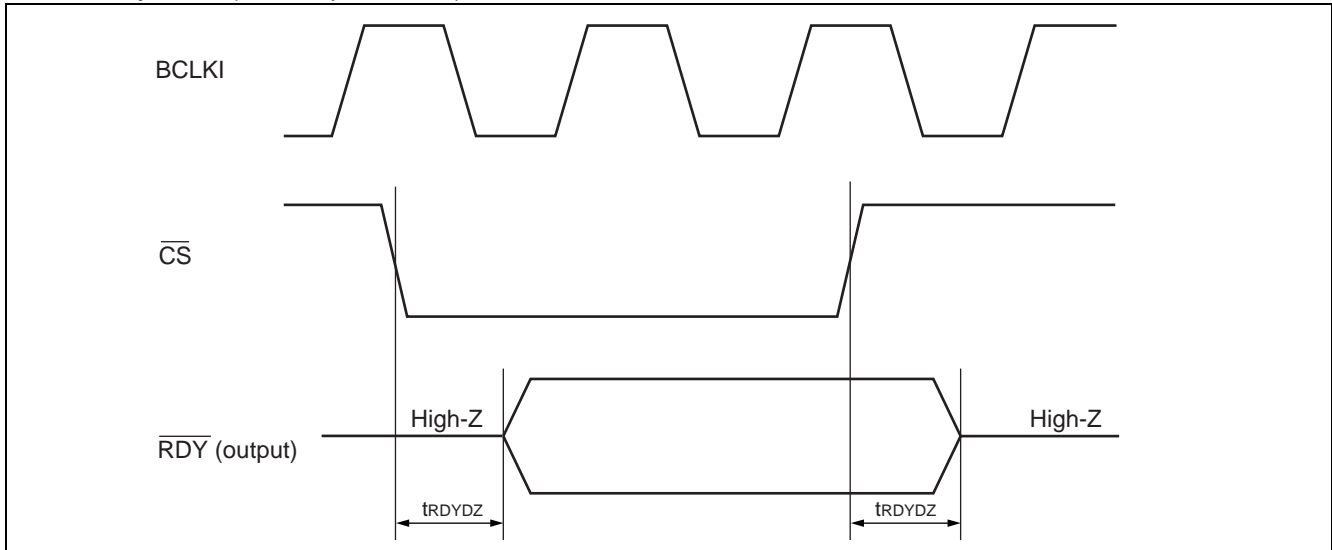


- DREQ output delay time

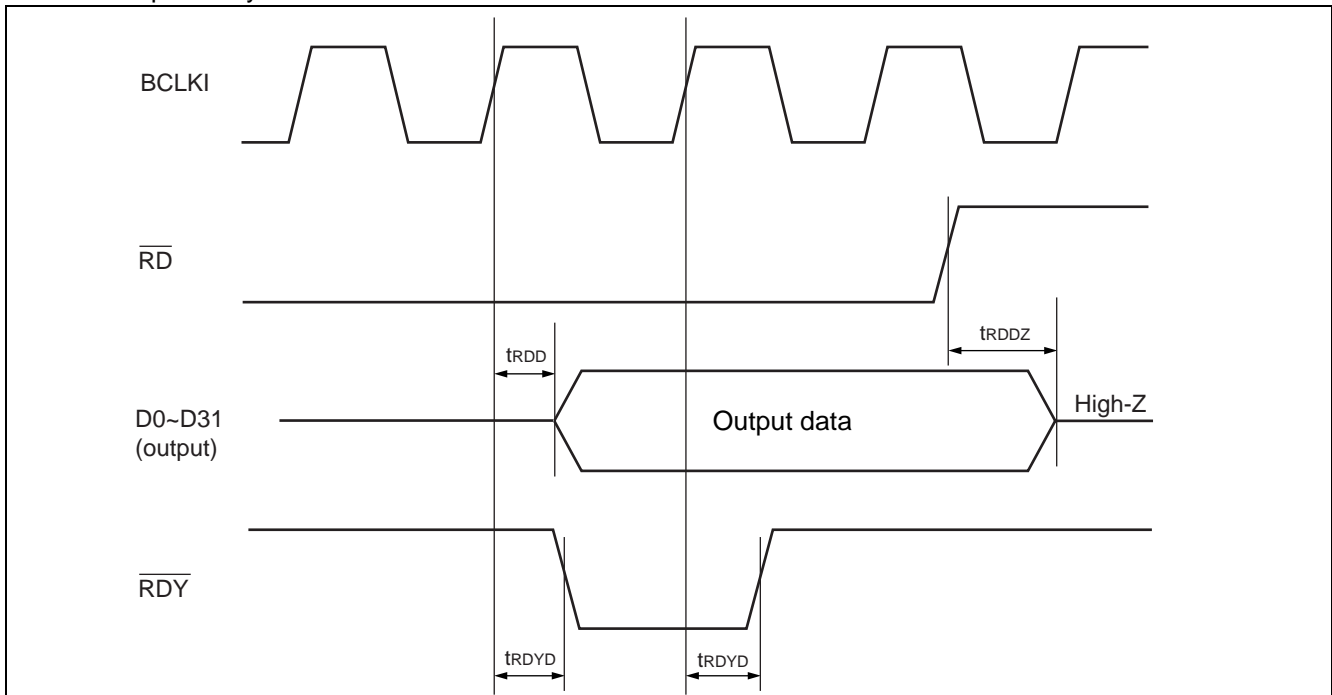


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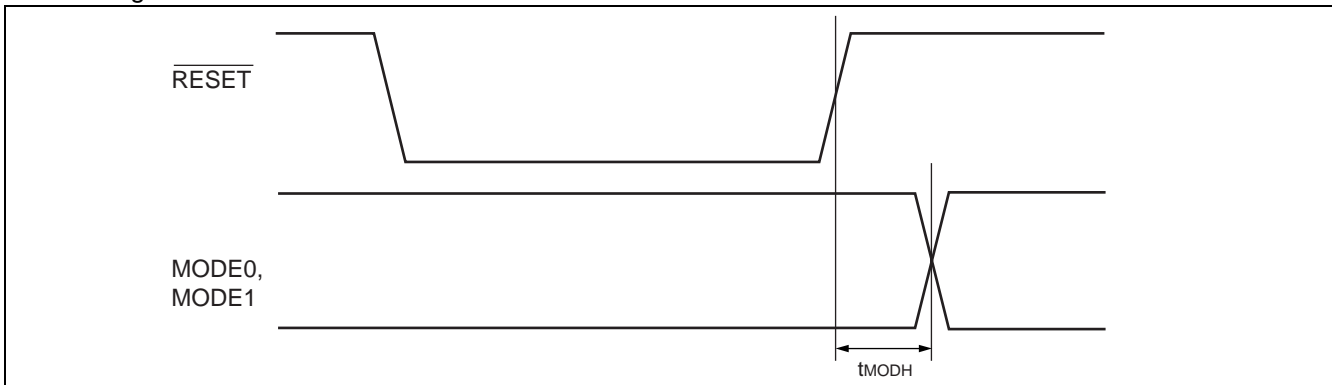
- $\overline{\text{RDY}}$  delay value (with respect to  $\overline{\text{CS}}$ )



- RDY/D output delay values



- MODE signal hold time



## (2) Video Interface

### • Clock

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
CLK frequency	$f_{CLK}$	—	—	14.32	—	MHz
CLK H period	$t_{HCLK}$	—	25	—	—	ns
CLK L period	$t_{LCLK}$	—	25	—	—	ns
DCLKI frequency	$f_{DCLKI}$	—	—	—	67	MHz
DCLKI H period	$t_{HDCLKI}$	—	5	—	—	ns
DCLKI L period	$t_{LDCLKI}$	—	5	—	—	ns
DCLKO frequency	$f_{DCLKO}$	—	—	—	67	MHz

### • Input signals

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
HSYNC input pulse width	$t_{WHSYNC0}$	*1	3	—	—	clock
	$t_{WHSYNC1}$	*2	3	—	—	clock
HSYNC input setup time	$t_{SHSYNC}$	*2	10	—	—	ns
HSYNC input hold time	$t_{HHSYNC}$	*2	10	—	—	ns
VSYNC input pulse width	$t_{WHSYNC1}$	—	1	—	—	HSYNC 1 cycle
EO input setup time	$t_{SEO}$	*3	10	—	—	ns
EO input hold time	$t_{HEO}$	*3	10	—	—	ns

\*1 : Applied only in PLL synchronization mode (CKS = 0) . The reference clock is the internal PLL's output with Cycle =  $1 / (14 f_{CLK})$  .

\*2 : Applied only in DCLKI synchronization mode (CKS = 1) . The reference clock is DCLKI.

\*3 : Based on the edge with VSYNC negated.

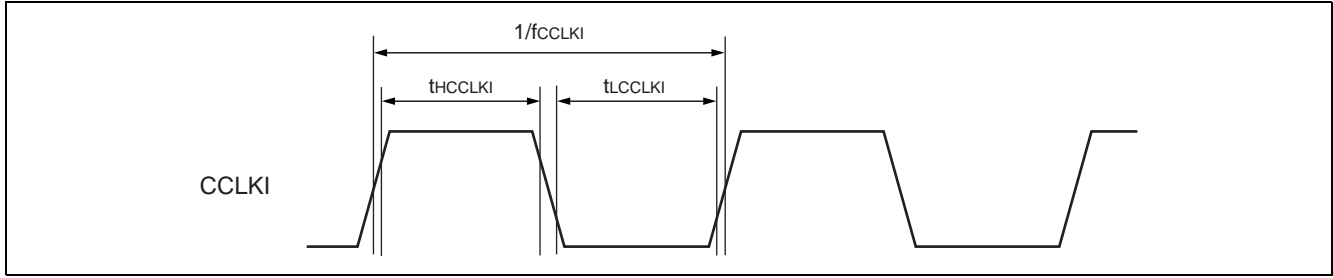
### • Output signals

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
EO output delay time	$t_{DEO}$	*	—	—	10	ns
HSYNC output delay time	$t_{DHSYNC}$	—	—	—	10	ns
VSYNC output delay time	$t_{DVSYNC}$	—	—	—	10	ns
CSYNC output delay time	$t_{DCSYNC}$	—	—	—	10	ns
GV output delay time	$t_{DGV}$	—	—	—	10	ns

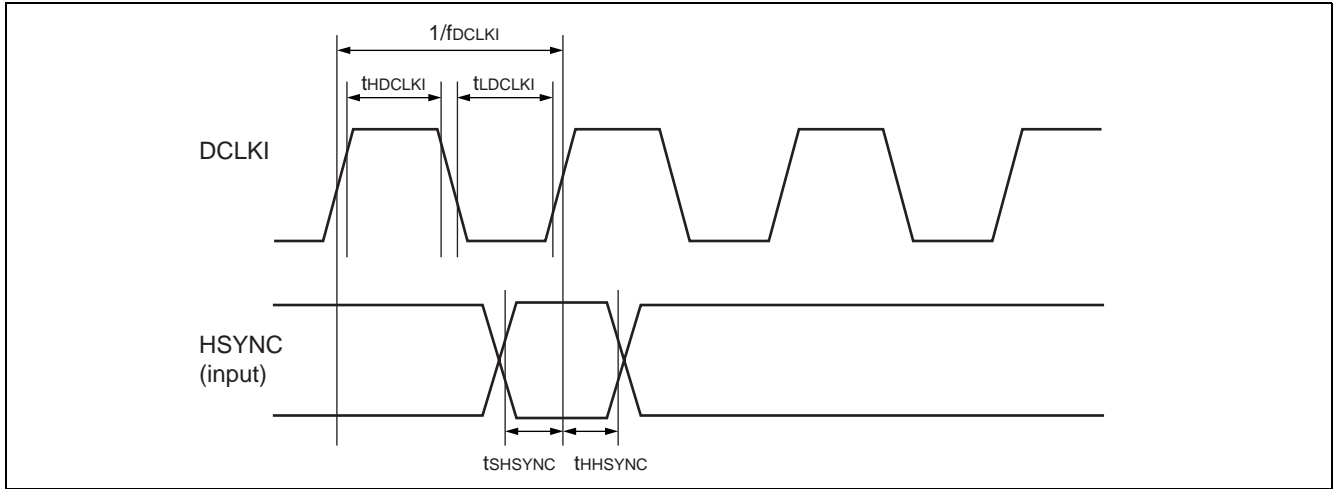
\* : The EO output varies at the same time as VSYNC is asserted.

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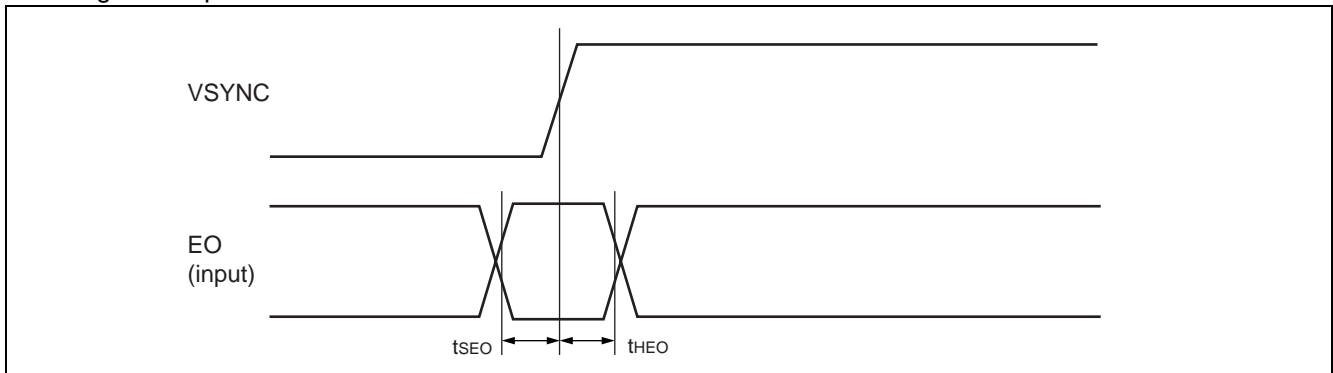
- Clock



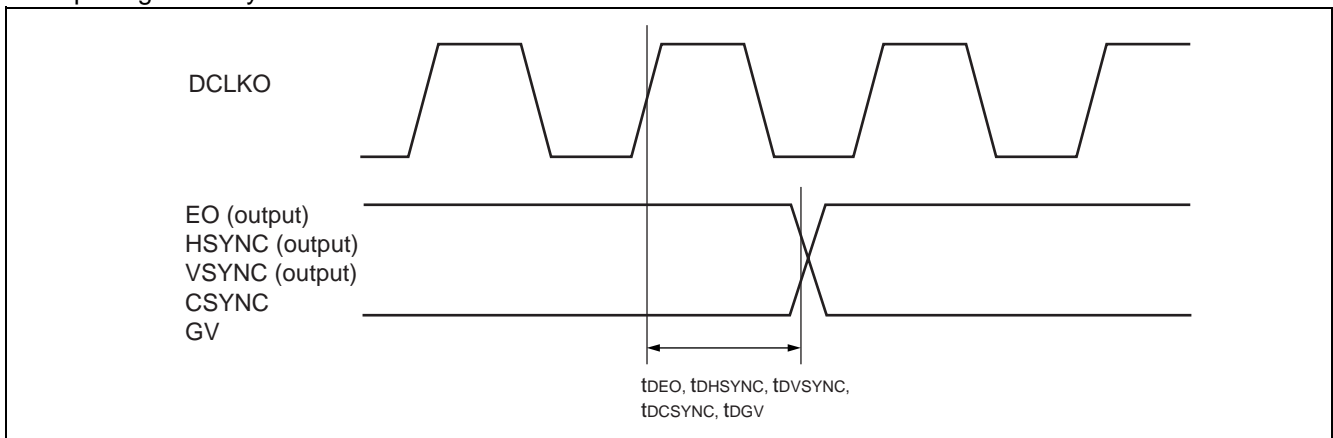
- HSYNC signal setup and hold



- EO signal setup and hold



- Output signal delay



## (3) Graphics Memory Interface

### • Clock

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
MCLKO frequency	f <sub>MCLKO</sub>	—	—	—	100	MHz
MCLKO H period	t <sub>HMCLKO</sub>	—	1	—	—	ns
MCLKO L period	t <sub>LMCLKO</sub>	—	1	—	—	ns
MCLKI frequency	f <sub>MCLKI</sub>	—	—	—	100	MHz
MCLKI H period	t <sub>HMCLKI</sub>	—	1	—	—	ns
MCLKI L period	t <sub>LMCLKI</sub>	—	1	—	—	ns
MCLKI delay to MCLKO	t <sub>OID</sub>	—	1	—	4	ns

### • I/O signals

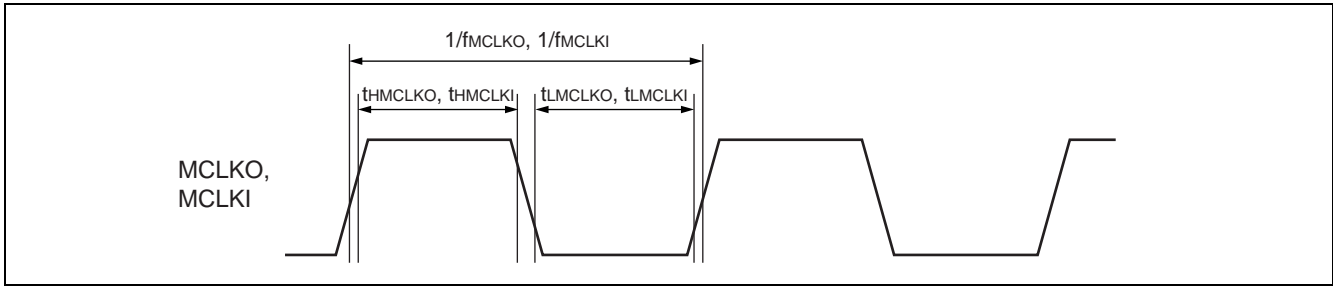
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
MA, MRAS, MCAS, MWE, CKE Setup time	t <sub>MADS</sub>	*1	3.5	—	—	ns
MA, MRAS, MCAS, MWE, CKE Hold time	t <sub>MADH</sub>	*1	1	—	—	ns
MDQM data setup time	t <sub>MDQMS</sub>	*1	3.5	—	—	ns
MDQM data hold time	t <sub>MDQMDH</sub>	*1	1	—	—	ns
MD output data setup time	t <sub>MDODS</sub>	*1	3.5	—	—	ns
MD output data hold time	t <sub>MDODH</sub>	*1	1	—	—	ns
MD input data setup time	t <sub>MDIDS</sub>	*2	3	—	—	ns
MD input data hold time	t <sub>MDIDH</sub>	*2	1	—	—	ns

\*1 : Setup/hold time with respect to MCLKO.

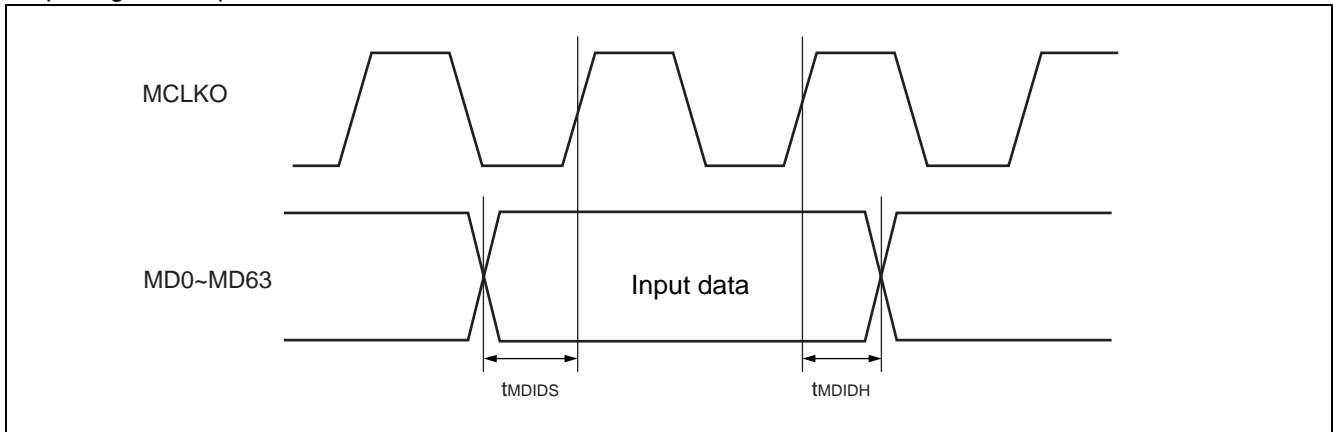
\*2 : Setup/hold time with respect to MCLKI.

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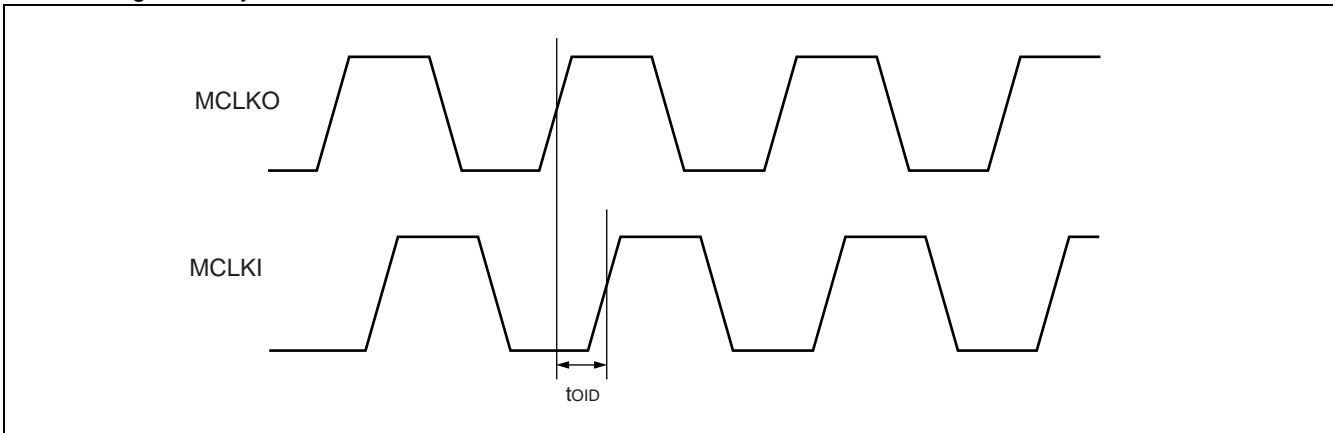
- Clock



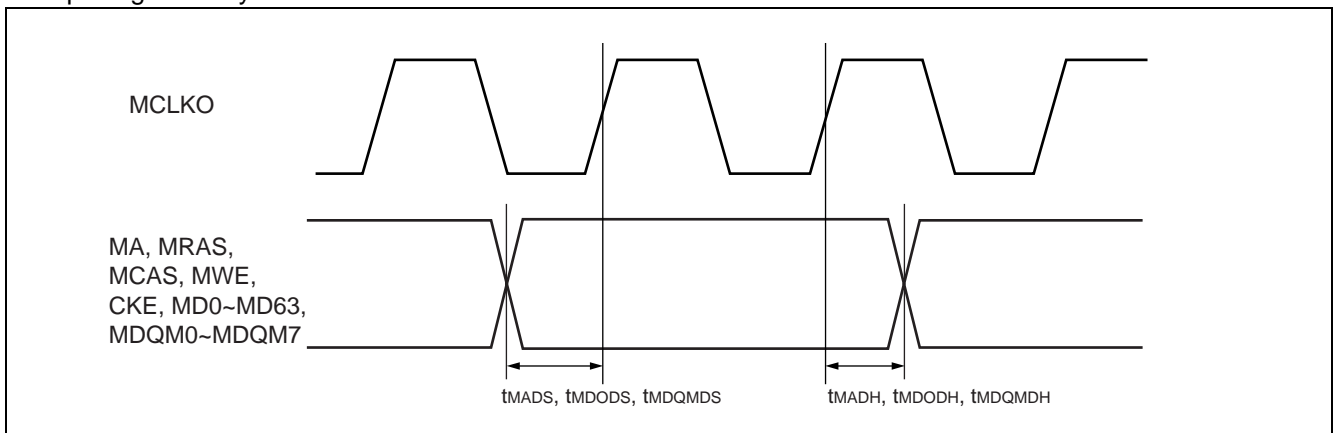
- Input signal setup and hold times



- MCLKI signal delay



- Output signal delay



## (4) PLL Standards

Parameter	Value			Unit	Description
	Min	Typ	Max		
Input frequency (Typical)	—	14.31818	—	MHz	
Output frequency	—	—	200.45452	MHz	Multiplied by 14
Duty ratio	93.1	—	101.3	%	PLL output clock H/L pulse width ratio
Jitter	- 150	—	+ 180	ps	Cycle difference between two consecutive cycles

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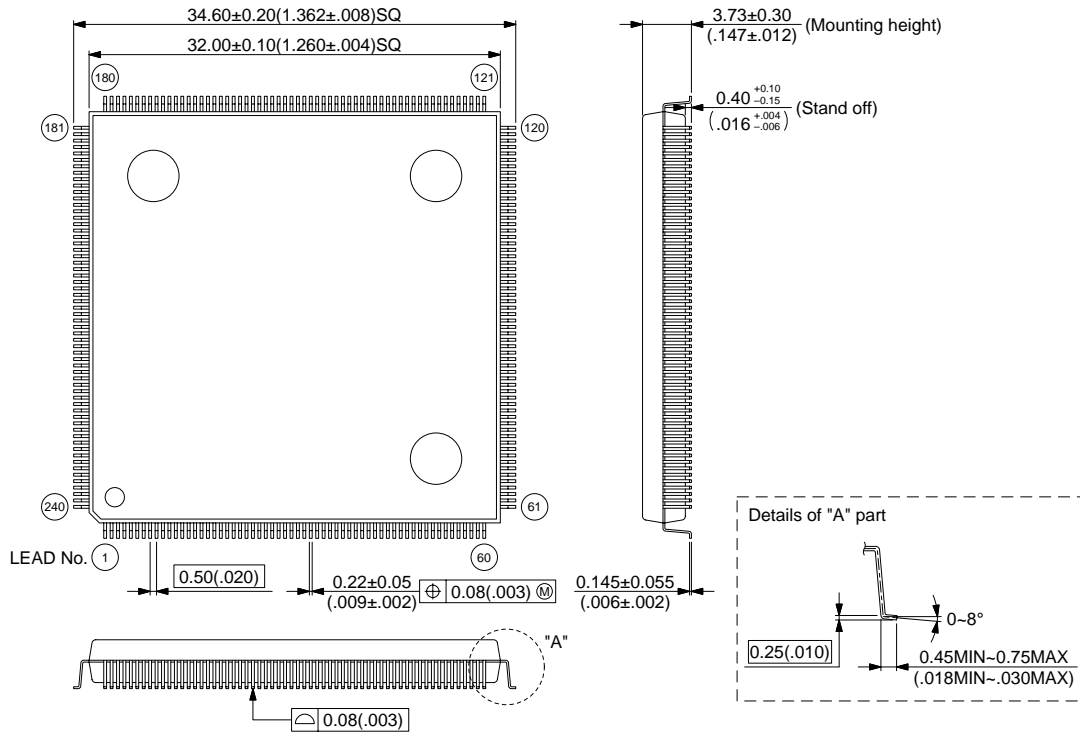
## ■ ORDERING INFORMATION

Part Number	Package	Remarks
MB86290APFVS	240-pin plastic QFP (FPT-240P-M03)	

## ■ PACKAGE DIMENSION

240-pin plastic QFP  
(FPT-240P-M03)

\*Pins width and pins thickness include plating thickness.



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Dimensions in mm (inches)

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