

MB8629XEB01

MB8629X Series Evaluation System
Hardware Specifications
Dec 24th 2003 (Rev. 1.1)



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1. Overview

This board is designed to mainly evaluate the functionality and performance of Fujitsu MB8629X Graphics Display Controller Series.

2. System Configuration

2.1 Board Configuration

This board uses with MB8629X series daughter board. Depending on the needs, this board can be used either by mounting on a PCI slot of ordinary Windows NT/2000 PC or by combining with a specific CPU evaluation board (A stand alone configuration). The applicable CPU boards are SH-3 EVA BOD(CX06706C-9901, SH3 CPU evaluation board) or SH-4 EVA BOD(CX06710B-9901, SH4 CPU evaluation board) made by Computex, or KZ-V832-01(V832 evaluation board) made by Kyoto Micro Computers, Co. Ltd. When you want to use this board with CPU board, you need MB8629XEBIF(connection board). And if you want to use this board with this V832 evaluation board, the dedicated interface adapter board “MB86290EB02” is needed too.

When MB8629XEB01 is mounted on a PCI slot, the PCI bus bridge device PCI9054(made by PLX) acts as a local bus master. When MB8629XEB01 is combined with a CPU board, the CPU itself mounted on that board takes this local bus master role.

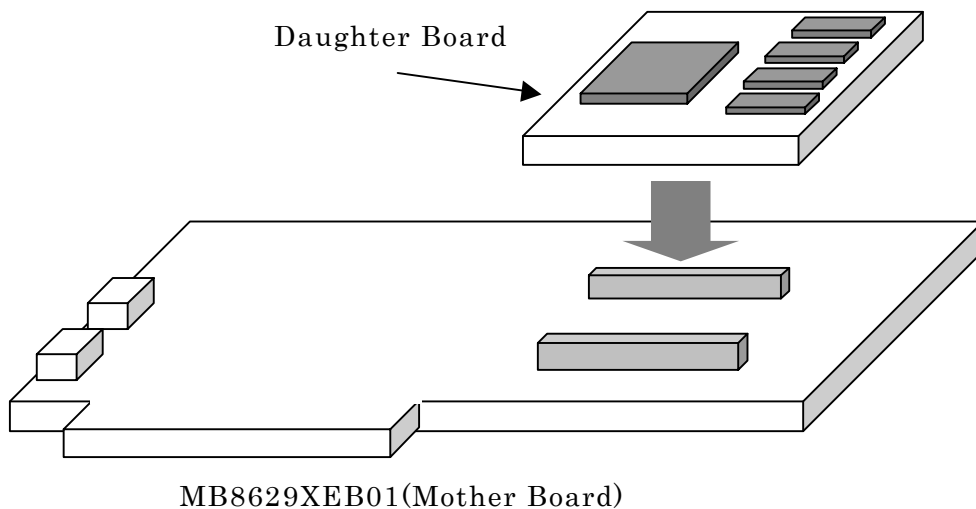


Fig 1. MB8629XEB01 Connection Diagram with Daughter Board

2.2 Component Outline

- PCI bridge
PCI9054 (made by PLX) and EEPROM [an equivalent 93CS56L]
- Video DAC ADV7120 (made by Analog Device)
- Digital Video Decoder SAA7113 (made by Philips)
- 8Bit DIP Switch
Read only
- 8Bit LED
Write only
- LED
Power on (Power supply indicator)
- CPU Board Interface Connector
100 pin half pitch x 3
- VGA Output Connector
Dsub15pin female connector
- VGA Input Connector for external sync
Dsub15pin female connector
- Composite Video Connector
Input connector x1
- Daughter Board Connection Connector
100 pin half pitch female connector x2

2.3 Power Supply

All of the power sources are supplied through interface connectors in either PCI bus mode or Local CPU board combination mode. And this board has power supply connectors which is able to supply the power.

Power connections on this board are as follows,

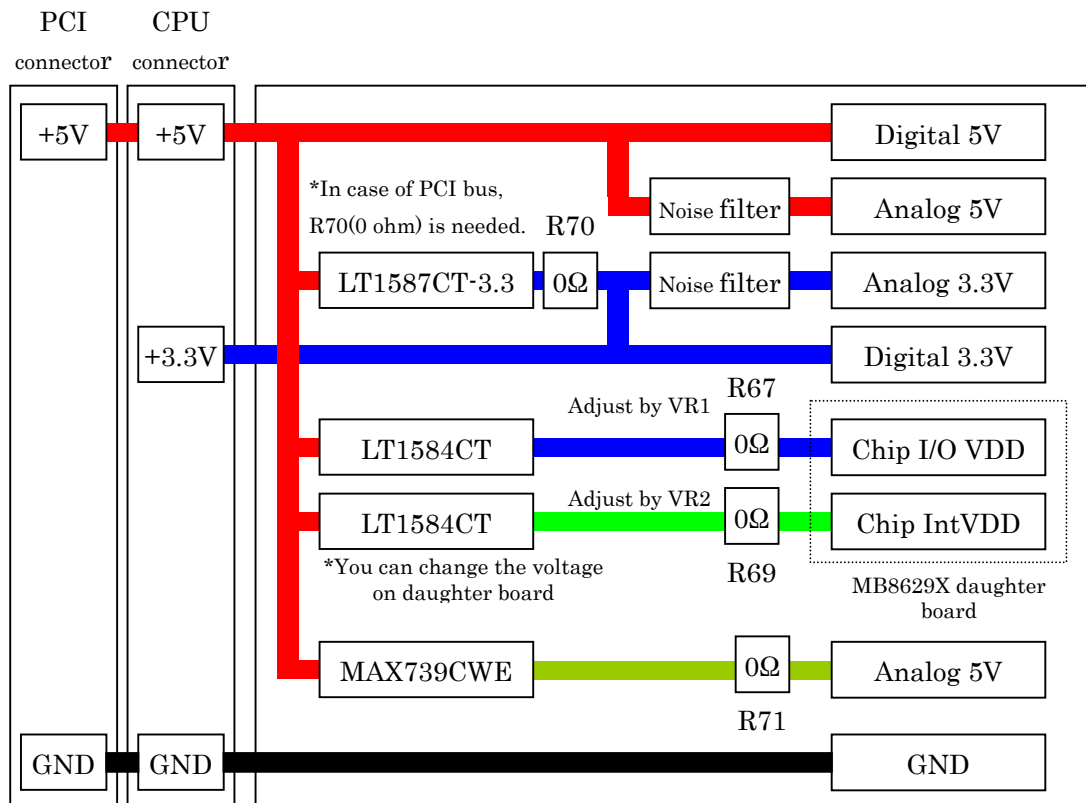


Fig 2-1. MB8629XE B01 Power supply Lines

3 Hardware Block Diagram

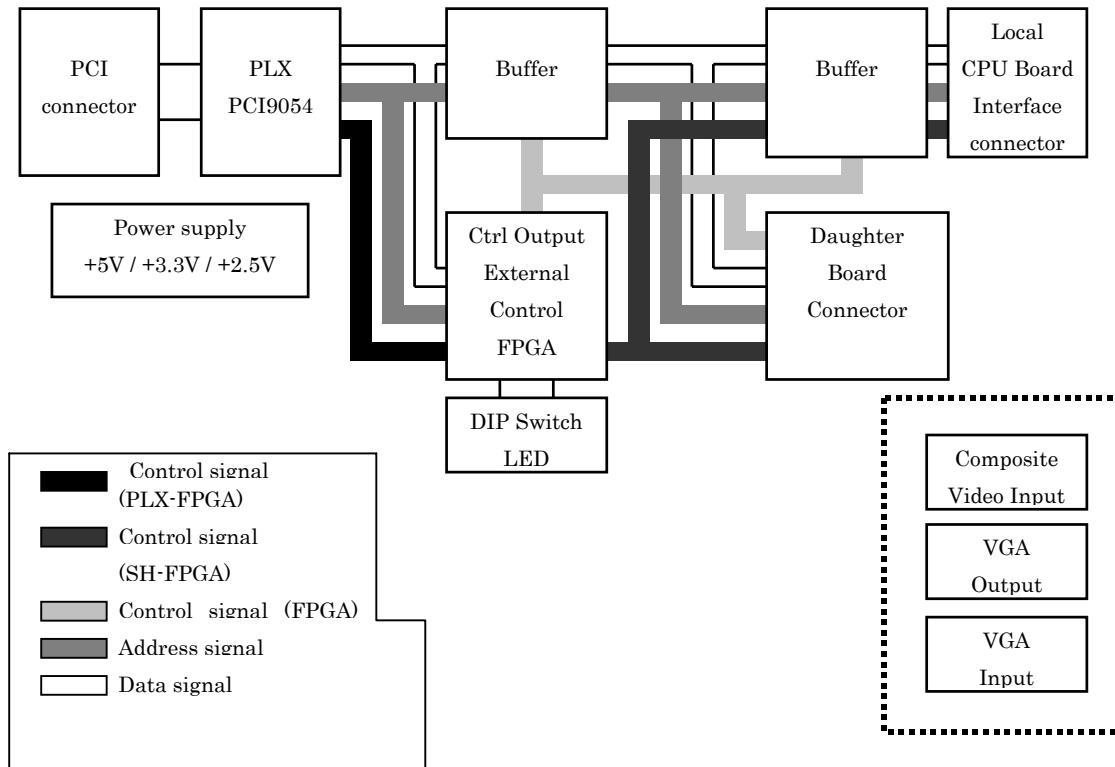


Fig 3-1. MB8629XEB01 Hardware Block Diagram

4 Memory Map

4.1 Memory Map in PCI bus access mode

The PCI Configuration ROM of MB8629X are the below.

- Vendor ID : 10b5
- Device ID : 9080

And the Base Address Registers are:

Base Address Register	Area Type	Range	Function
BADDR0	Memory	256byte	Local Register Area of PLX9054
BADDR1	IO	256byte	Reserved
BADDR2	Memory	128Mbyte	Daughter Board and FPGA Area
BADDR3	Memory	16Mbyte	Reserved

The memory map of BADDR2 is the below.

000 0000h	Daughter Board Area (Coral chip area)	32bit	PCI Local Address Space 0
3FF FFFFh			
400 0000h	Reserved	32bit	
400 0FFFh			
400 1000h	FPGA	32bit	
400 1FFFh	Internal Register Area		

Table 4-1. MB8629XE01 Memory Map (PCI bus access mode)

4.2 Memory Map in Local CPU access mode

1000 0000h 13FF FFFFh	MB8629X Daughter Board Area	32bit	SH_CS4
1400 0000h 1400 0FFFh	PLX PCI9054 Internal Register Area	32bit	SH_CS5 &A12=0
1400 1000h 1400 1FFFh	FPGA Internal Register Area	32bit	SH_CS5 &A12=1

Table 4-2. MB8629XEB01 memory map (Local CPU access mode)

4.3 Register Map

Device	Register	Address	Access	Data Size	True State	R/W
LEDR	LED Register	0x1400 1000	32bit	7:0	1=Light	RW
CTLR	Control Register	0x1400 1004	32bit	7:0	1	RW
DIPSWR	DIP Switch Register	0x1400 1008	32bit	7:0	Off=1	RO
OPSWR	Option Switch Register	0x1400 100C	32bit	7:0	Off=1	RO

Table 4-3. MB8629XEB01 Register map

4.4 Board Configuration Register

Name :CTRL
Address :1400 1004H
Mode :Read / Write

Bit	Name	Function	0	1
D4	IMASK	Mask Interrupt (PCI bus access mode)	Disable MB8629X interrupt signal (Default)	Enable MB8629X Interrupt signal
D0	ESE	External sync Enable	Disable	Enable the external Even/Odd signal input to MB8629X in External sync mode

Table 4-4. Board Configuration Register Bit Assignment

5 External Appearance

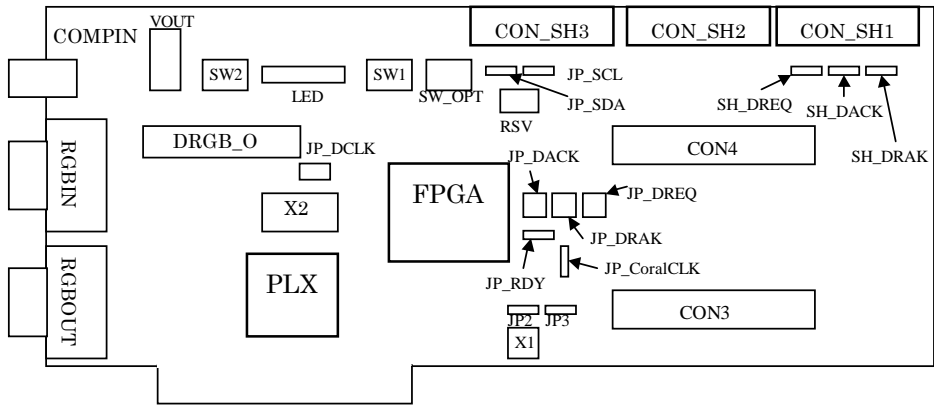


Fig 5-1. MB8629XEB01 External Appearance

5.1 Switch Settings

Switch	Function	Set	Description
SW1-1-8	DIP Switch	ON	ALL OFF
		OFF	
SW2-1	Set GV signal (Valid when JP_GV is 1-2)	ON	GV=L(Select Video input)
		OFF	GV=H(Select MB8629X) (Default)
SW2-2	Set AV9173-01(Video Genlock PLL) FS0 pin	ON	DCLK Freq=10 to 75 MHz(Default)
		OFF	DCLK Freq=2.5 to 18.75 MHz
SW2-3	ADV7120(Video DAC) Set BLANK pin	ON	Output Analog RGB Blank Revel (Degital RGB input, Ignore REF_WHITE)
		OFF	Output Analog RGB D/A Convert Signal (Default)
SW2-4	ADV7120(Video DAC) Set REF_WHITE pin	ON	Output Analog RGB D/A Convert Signal (Default)
		OFF	Output Analog RGB White Revel (Ignore Digital RGB input)
SW2-5,6	Reserved		
SW2-7	PCI9054 Input TEST pin	ON	Normal mode(Default)
		OFF	PCI9054 Test Mode
SW2-8	PCI9054 Input BIGEND#pin	ON	Set Local Bus Big Endian
		OFF	Set Local Bus Little Endian(Default)
SW_OPT1, 3-7	Reserved		
SW_OPT-2	Set Access Mode	ON	Local CPU Mode
		OFF	PCI Mode(Default)
SW_OPT-8	Set DOTCLK	ON	NTSC Mode
		OFF	VGA Mode(Default)
SW_RST	RESET Input		

Table 5-1. MB8629XEB01 Switch settings

5.2 Jumper settings

Jumper	Function	Set	Description
JP_CRGB, JP_RGB	Select RGB output	JP-CRGB:1-2 JP-RGB:1-2	Select AVD7120(DAC) Output
		JP-CRGB:1-2 JP-RGB:2-3	Select EL4331(Video SW) Output The source RGB are AVD7120 and External RGB(Default)
		JP-CRGB:2-3 JP-RGB:1-2	Select Analog RGB form Daughter Board
		JP-CRGB:2-3 JP-RGB:2-3	Select EL4331(Video SW) Output The source RGB are Analog RGB form Daughter Board and External RGB
JP_GV	EL4331(Video SW) Select Control Signal	1-2	Valid SW2-1(Refer SW2-1) (Default)
		2-3	Valid MB8629X's GV Signal
JP_ CORALCLK	MB8629X Select Bus Clock Input	1-2	Clock Input Normally(Default)
		2-3	Opposite Clock Input
JP_RDY	Ready pin of MB8629X Select Pull-Up/Down	1-2	Pull-Up
		2-3	Pull-Down
		Open	Nothing Pull-Up/Down(Default)
JP_SCL	Select SCL Signal for I2C I/F	1-2	Reserved(Default)
		2-3	Reserved
JP_SDA	Select SDA Signal for I2C I/F	1-2	Reserved(Default)
		2-3	Reserved
JP_SHDACK	Select DACK Signal of Local CPU Mode	1-2	Select DACK0
		2-3	Select DACK1(Default)
JP_SHDRAK	Select DRAK Signal of Local CPU Mode	1-2	Select DRAK0
		2-3	Select DRAK1(Default)
JP_SHDREQ	Select DREQ Signal of Local CPU Mode	1-2	Select DREQ0
		2-3	Select DREQ1(Default)
JP_DACK	Select DACK Signal	2-4	Fixed(Default)
JP_DRAK	Select DRAK Signal	2-4	Fixed(Default)
JP_DREQ	Select DREQ Signal	2-4	Fixed(Default)
CON_DCLK	Select DCLKI	1-2 Short	Select PLL Output DOTCLK(Default)
		3-4 Short	Select Opposite PLL Output DOTCLK
		5-6 Short	Select X2 Clock(NOT Mounted)
		7-8 Short	Fixed Low Revel
		JP:Open 2,4,6,8 pin: Input External CLK	Select External CLK Input

Table 5-2. MB8629XEB01 Jumper Settings(1)

Jumper	Function	Set	Description
JP1	Select X1(Crystal) 1 pin (OE Control Device)	Short	1pin = VDD5(Default)
		Open	1pin = Open
JP2,3	Select Bus Clock	JP2:1-2,JP3:2-3	PCI Mode Select X1(Crystal)(Default)
		JP2:2-3,JP3:2-3	PCI Mode Select CCLK of SAA7113
		JP2:Don't Care JP3:1-2	Local CPU Mode
		Others	Reserved

Table 5-3. MB8629XEB01 Jumper Settings (2)

5.3 Change PCI mode or Local CPU mode

The switch and jumper settings for PCI bus mode or Local CPU board mode are follows:
 Default is set to PCI bus mode.

Mode	SW_OPT-2	SW2-7	JP3
PCI bus mode	OFF	ON	2-3
Local CPU board mode	ON	OFF	1-2

Table 5-4 Settings for PCI mode or Local CPU mode

5.4 The Connector for Local CPU Interface Board

This board has three special connectors to interface to local CPU board (SH3:SH7709A and SH4:SH7750 are the expected host CPU for this board).

Using Local CPU Connection Board(MB8629XEBIF), this board is able to connect directly with Local CPU board.

Note) The interrupt signal from MB8629X is connected to IRL2 and IRL3 signal of SH connector through FPGA.

Status of Scarlet Interrupt signal	Status of IRL[3:0] in SH connector
Low(Interrupt)	0x3
High(No Interrupt)	0xf

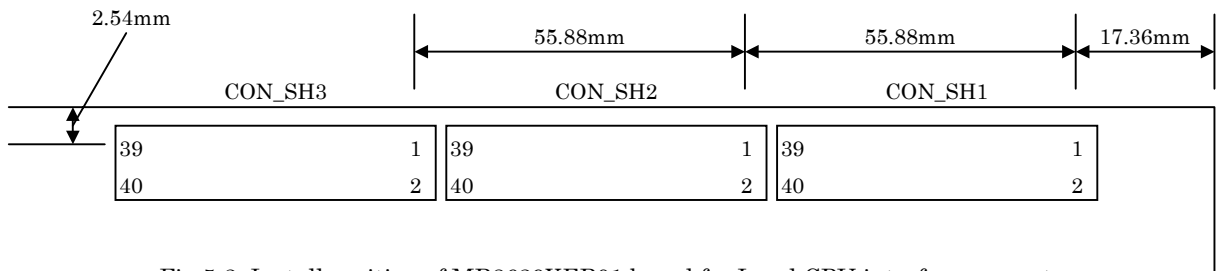


Fig 5-2. Install position of MB8629XEB01 board for Local CPU interface connector

<Using connector (CON_SH1~CON_SH3)>
 Pin pitch 2.54mm, 2Lines x 20pin header

<Part Number of these connector>
 PS-40SD-D4TS1-1 (made by JAE)

Signal Pin Assignment for Local CPU Interface board

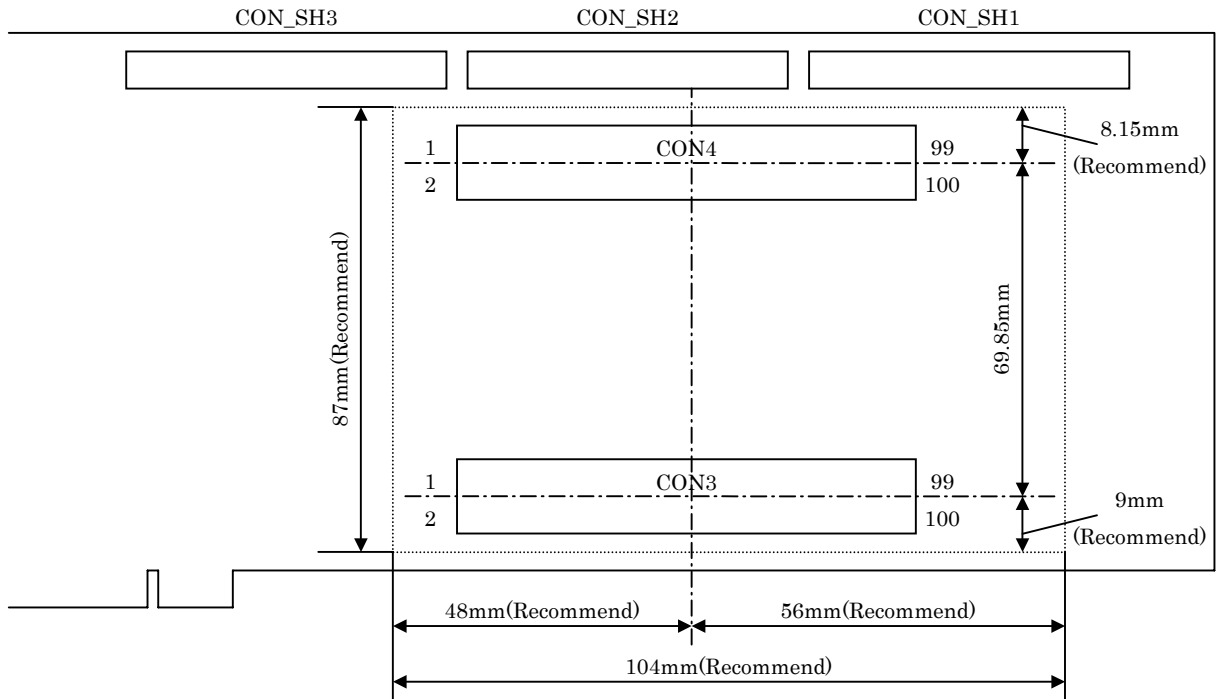
CON_SH1				CON_SH2			
1	~CS0	2	~WE0	1	VDD5	2	VDD3
3	~CS1	4	~WE1	3	A2	4	A3
5	~CS2	6	~WE2	5	A4	6	A5
7	~CS3	8	~WE3	7	A6	8	A7
9	VDD5	10	VDD3	9	VDD5	10	VDD3
11	~CS4	12	RDWR	11	A8	12	A9
13	~CS5	14	~BS	13	A10	14	A11
15	~CS6	16	GND	15	A12	16	A13
17	~RD	18	CKIO	17	A14	18	A15
19	GND	20	GND	19	GND	20	GND
21	~IRL0	22	~IRL1	21	A16	22	A17
23	~IRL2	24	~IRL3	23	A18	24	A19
25	~RESETOUT	26	RDY	25	A20	26	A21
27	~BACK	28	~BREQ	27	A22	28	A23
29	VDD5	30	VDD3	29	VDD5	30	VDD3
31	DRAK1	32	DRAK0	31	A24	32	A25
33	~DREQ0	34	DACK0	33	VDD5	34	VDD3
35	~DREQ1	36	DACK1	35	GND	36	GND
37	GND	38	GND	37	GND	38	GND
39	GND	40	GND	39	GND	40	GND

CON_SH3			
1	D0	2	D1
3	D2	4	D3
5	D4	6	D5
7	D6	8	D7
9	VDD5	10	VDD3
11	D8	12	D9
13	D10	14	D11
15	D12	16	D13
17	D14	18	D15
19	GND	20	GND
21	D16	22	D17
23	D18	24	D19
25	D20	26	D21
27	D22	28	D23
29	VDD5	30	VDD3
31	D24	32	D25
33	D26	34	D27
35	D28	36	D29
37	D30	38	D31
39	GND	40	GND

Table 5-5. Connectors pin assignment for Local CPU Interface board

5.5 The Connector for Daughter Board

This board has two connector for connecting to daughter board(GDC mounted board).
 Follows are a size of connector and pin assignment.



Note) The size of connector is the center via the center size of each parts.
 [Recommend] is a size of daughter board.

<Connector (CON3,CON4)>
 8903-100-177MS-A (Made by KEL)

<Connector for Daughter Board (Reference)>
 8913-100-178MS-A (Made by KEL)

<Recommended Daughter Board Size>
 87mm x 104mm

Signal Pin Assignment of the Connector for Daughter Board

CON3				CON4			
1	DB_VDD3	2	DB_VDDL	1	DB_VDD3	2	DB_VDDL
3	A2	4	A3	3	DB_VDD3	4	DB_VDDL
5	A4	6	A5	5	DB_VDD3	6	DB_VDDL
7	A6	8	A7	7	R7	8	R6
9	GND	10	GND	9	R5	10	R4
11	A8	12	A9	11	R3	12	R2
13	A10	14	A11	13	R1	14	R0
15	A12	16	A13	15	GND	16	GND
17	A14	18	A15	17	GND	18	GND
19	DB_VDD3	20	DB_VDDL	19	GND	20	GND
21	A16	22	A17	21	G7	22	G6
23	A18	24	A19	23	G5	24	G4
25	A20	26	A21	25	G3	26	G2
27	A22	28	A23	27	G1	28	G0
29	GND	30	GND	29	DB_VDD3	30	DB_VDDL
31	A24	32	A25	31	DB_VDD3	32	DB_VDDL
33	DB_VDD3	34	DB_VDDL	33	DB_VDD3	34	DB_VDDL
35	~WE3	36	~WE2	35	B7	36	B6
37	~WE1	38	~WE0	37	B5	38	B4
39	GND	40	GND	39	B3	40	B2
41	GND	42	~DTACK	41	B1	42	B0
43	~DRACK	44	BSMODE	43	GND	44	DB_VDDL
45	RDYMODE	46	~INT	45	GND	46	DB_VDDL
47	~DREQ	48	~RDY	47	AOUTR	48	AOUTG
49	DB_VDD3	50	DB_VDDL	49	GND	50	AOUTB
51	CLK	52	~CS	51	S	52	GND
53	~RD	54	~BS	53	TRST	54	DCLKI
55	MODE0	56	MODE1	55	DB_VDD3	56	GND
57	MODE2	58	~RESET	57	DB_VDD3	58	N.C.
59	GND	60	GND	59	DB_VDD3	60	DB_VDDL
61	D0	62	D1	61	SCL	62	SDA
63	D2	64	D3	63	VSYNC	64	HSYNC
65	D4	66	D5	65	CSYNC	66	GV
67	D6	68	D7	67	DE	68	DCLKO
69	DB_VDD3	70	DB_VDD3	69	GND	70	GND
71	D8	72	D9	71	GND	72	GND
73	D10	74	D11	73	GND	74	GND
75	D12	76	D13	75	DV_VPO7	76	DV_VPO6
77	D14	78	D15	77	DV_VPO5	78	DV_VPO4
79	GND	80	GND	79	DV_VPO3	80	DV_VPO2
81	D16	82	D17	81	DV_VPO1	82	DV_VPO0
83	D18	84	D19	83	DV_CCLK	84	DB_VDD3
85	D20	86	D21	85	DB_VDD3	86	DB_VDD3
87	D22	88	D23	87	DB_VDD3	88	DB_VDD3
89	DB_VDD3	90	DB_VDD3	89	N.C.	90	N.C.
91	D24	92	D25	91	VDD5	92	VDD5
93	D26	94	D27	93	N.C.	94	N.C.
95	D28	96	D29	95	GND	96	GND
97	D30	98	D31	97	GND	98	GND
99	GND	100	GND	99	GND	100	GND

5.6 Signal Pin Assignment of Digital RGB Output

CON_RGBOUT			
1	R0	2	R1
3	R2	4	R3
5	R4	6	R5
7	R6	8	R7
9	GND	10	GND
11	G0	12	G1
13	G2	14	G3
15	G4	16	G5
17	G6	18	G7
19	GND	20	GND
21	B0	22	B1
23	B2	24	B3
25	B4	26	B5
27	B6	28	B7
29	GND	30	GND
31	ORC_HSYNC	32	ORC_VSYNC
33	ORC_CSYNC	34	ORC_DE
35	DCLKO	36	N.C.
37	N.C.	38	N.C.
39	N.C.	40	GND

Table 5-6 Pin Assignment for Digital RGB

5.7 Signal Pin Assignment of Analog RGB Input for External Sync

CON_RGBIN					
1	EXTIN_R	6	GND	11	N.C.
2	EXTIN_G	7	GND	12	N.C.
3	EXTIN_B	8	GND	13	EXT_HSYNC
4	N.C.	9	N.C.	14	EXT_VSYNC
5	GND	10	GND	15	N.C.

Table5-7 Pin Assignment of Analog RGB Input for External Sync

5.8 Signal Pin Assignment of Digital Video Decoder Output

CON_VOUT			
1	VPO0	2	VPO1
3	VPO2	4	VPO3
5	VPO4	6	VPO5
7	VPO6	8	VPO7
9	CCLK	10	GND

Table5-8 Pin Assignment of Digital Video Decoder Output

6 Appendix

6.1 Interrupt to PCI bus

To assert an interrupt to PCI bus, set registers as the below.

- Set IMASK register (Interrupt Mask register, BADDR2+HostBase+0x24) in Coral.
(All of interrupt factors are masked in default)
- Set bit4 of CTRL register (BADDR2+0x4001004) in FPGA to "1".
- Set bit11 and bit8 of ISTCSR register (BADDR0+0x68) in PLX9054 to "1".

The interrupt status are seen by the below registers.

- Bit15 of INTCSR register in PLX9054. If this bit set to "1", the interrupt from Coral is occurred.
- IST (Interrupt status, BADDR2+HostBase+0x20) in Coral

Note)

1. INTCSR register (Default = 0x0f010100)
The function of each bits are the below.

Bit8 : PCI interrupt enable =>Enable an interrupt to PCI bus. 1=Enable.

Bit11 : Local interrupt input enable=>Enable an interrupt from Coral, 1=Enable

Bit15 : Local input interrupt active=>The interrupt status form Coral, 1=Interrupt

2. The driver for PC

The driver (Map Driver) which we attach the evaluation board for PC (Windows) does NOT support the interrupt.