

MB86294EB01

Coral-LB[MB86294/294S]Evaluation System
Hardware Specifications
December 26 2002 (Rev. 1.0)



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1. Overview

This board is designed to mainly evaluate the functionality and performance of Fujitsu MB86294/294S[Coral-LB] Graphics Display Controller.

2. System Configuration

2.1 Board Configuration

You need MB8629XEB01(Mother board) to use this board. This board work as daughter board.

The connection between MB86294EB01(daughter board) and MB8629XEB01(mother board) is below.

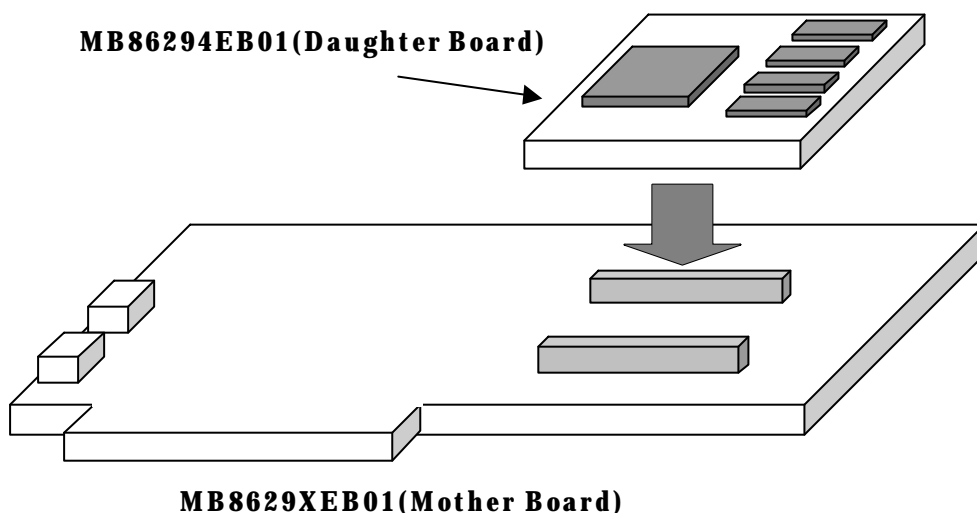


Fig 1. MB86294EB01 Connection Diagram with MB8629XEB01

Note)

If you don't evaluate "external sync", please set jumper and switch on MB8629XEB01 (Mother board) to follows.

JP_CRGB_1,2,3,4	: 2 - 3 (Select Coral-LB's DAC output)
JP_RGB_1,2,3,4	: 2 - 3 (Select Video Switch output)
JP_GV	: 1 - 2 (Select "Switch signal" of Video Switch to SW2-1)
JP_SCL,JP_SDA	: 1 - 2
SW2-1	: OFF (Select MB86293 output)

And the MB86294EB01 were set to video capture input mode(memory bus width 32bit) in default.

2.2 Component Outline

■ **Coral_LB**

MB86294S (Graphics Display Controller with I²C interface*1)

■ **SDRAM W982516BH** (made by Winbond)

256Mbit x16 SDRAM x 4pcs

■ **MB8629XEB01(Mother Board) Connection Connector**

100 pin half pitch female connector x2

Note:

*1: Purchase of Fujitsu FC components conveys a license under the Philips FC Patent Right to use these components to the I²C Standard Specification as defined by Philips.

*2: There is two type of Coral-LB, one(MB869294S) with the I²C interface and the other one(MB86924) without it. And MB86294S is mounted on this board.

2.3 Power Supply

All of the power sources are supplied from MB8629XEB01(Mother Board).A voltage can adjust by a volume on the Mother Board. Please refer "MB8629XEB01 Spec Sheet".

3 External Appearance

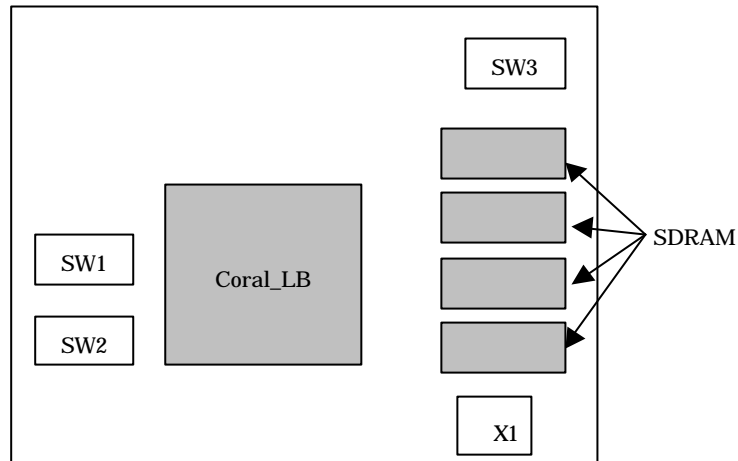


Fig 3-1. MB86294EB01 External Appearance

3.1 Switch Settings

Switch	Function	Set	Description
SW1-1-5	Coral_LB Input TESTH pin	ON=L	ALL OFF
		OFF=H	
SW1-6	Coral_LB Set Clock Mode(CKM pin)	ON	Select PLL output(Default)
		OFF	Select Host CPU bus clock
SW1-7,8	Coral_LB Set CLKSEL pin (Valid SW1-6 ON)	Bit7,8	Note)1=OFF,0=ON
		0,0	Input 13.5MHz
		0,1	Input 14.32MHz(Default)
		1,0	Input 17.73MHz
		1,1	Reserved
SW2-1-3	Coral_LB Set CPU Mode (MODE0-2 pin)	Bit1,2,3	Note)1=OFF,0=ON,x=Don't Care
		0,0,0	SH3 Mode
		0,0,1	SH4 Mode(Default)
		0,1,0	V83x Mode
		0,1,1	Sparc lite Mode
		1,X,X	Reserved
SW2-4	Coral_LB Set BS Mode(BS_MODE pin)	ON	Connect CPU with BS signal(Default)
		OFF	Connect CPU without BS signal
SW2-5	Coral_LB Set RDY Mode(RDY_MODE pin)	ON	Normally Not Ready(Default)
		OFF	Normally Ready
SW2-6	Coral_LB Set XRGBEN	ON	SDRAM 32bit, video capture on(Default)
		OFF	SDRAM 64bit, video capture off
SW2-7	Reserved		
SW2-8	Set BS Signal Supply	ON	Supply BS Signal(Default)
		OFF	Not Supply BS Signal
SW3-1-7	Set Graphics Memory Type	Bit1-7	0=ON,1=OFF
		1,1,0,1,1,1,1	FCRAM 16Mbit 2bank
		0,1,1,0,1,0,1	SDRAM 64/128Mbit 2/4bank
		0,0,1,1,0,1,0	SDRAM 256Mbit 4bank(Default)
		Others	Reserved
SW3-8	Reserved		

Table 3-1. MB86294EB01 Switch settings

3.2 Select PCI mode or Local CPU mode

The switch and jumper settings for PCI bus mode or Local CPU board mode are follows:
Default is set to PCI bus mode.

Mode	SW2-5
PCI bus mode	ON Normally Not Ready
Local CPU board mode	OFF Normally Ready

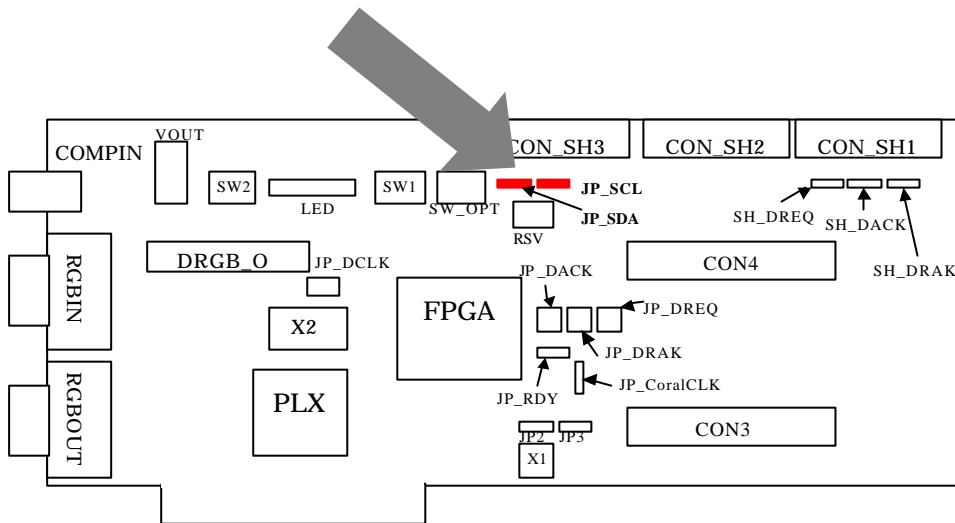
Table 3-3 Settings for PCI mode or Local CPU mode

3.3 Use the video capture function

The video capture pins of Coral-LB are multiplexed with graphics memory interface pins. And Coral-LB has to control video encoder LSI on the mother board. Therefore please set jumper and switch as the follows when you evaluate video capture function. And please be aware that you have to set MMR(memory mode register) to 32bit mode(0x014eb813).

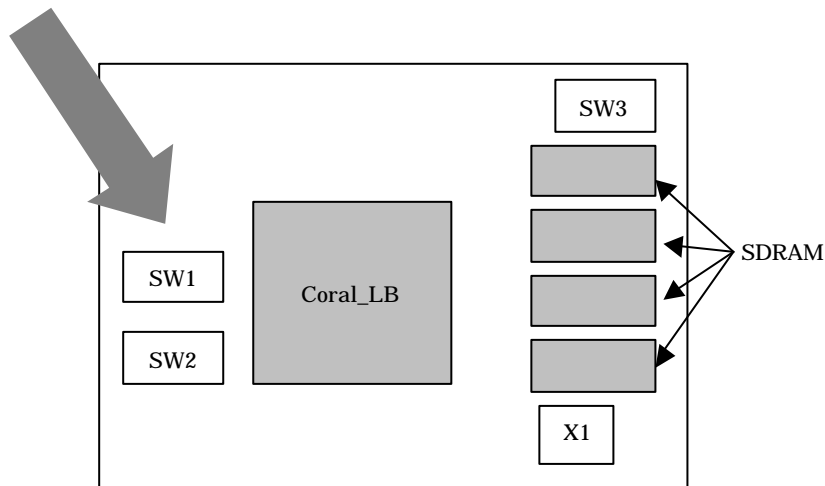
MB8629XE01(Mother Board)

JP_SCL:1-2, JP_SDA:1-2



MB86294EB01(Daughter Board)

SW2-6:ON



Signal Pin Assignment of the Connector for MB8629XE01

CON1				CON2			
1	DB_VDD3	2	DB_VDDL	1	DB_VDD3	2	DB_VDDL
3	A2	4	A3	3	DB_VDD3	4	DB_VDDL
5	A4	6	A5	5	DB_VDD3	6	DB_VDDL
7	A6	8	A7	7	R7	8	R6
9	GND	10	GND	9	R5	10	R4
11	A8	12	A9	11	R3	12	R2
13	A10	14	A11	13	R1	14	R0
15	A12	16	A13	15	GND	16	GND
17	A14	18	A15	17	GND	18	GND
19	DB_VDD3	20	DB_VDDL	19	GND	20	GND
21	A16	22	A17	21	G7	22	G6
23	A18	24	A19	23	G5	24	G4
25	A20	26	A21	25	G3	26	G2
27	A22	28	A23	27	G1	28	G0
29	GND	30	GND	29	DB_VDD3	30	DB_VDDL
31	A24	32	A25	31	DB_VDD3	32	DB_VDDL
33	DB_VDD3	34	DB_VDDL	33	DB_VDD3	34	DB_VDDL
35	~WE3	36	~WE2	35	B7	36	B6
37	~WE1	38	~WE0	37	B5	38	B4
39	GND	40	GND	39	B3	40	B2
41	GND	42	~DTACK	41	B1	42	B0
43	~DRACK	44	BSMODE	43	GND	44	DB_VDDL
45	RDYMODE	46	~INT	45	GND	46	DB_VDDL
47	~DREQ	48	~RDY	47	Reserved	48	Reserved
49	DB_VDD3	50	DB_VDDL	49	GND	50	Reserved
51	CLK	52	~CS	51	S	52	GND
53	~RD	54	~BS	53	TRST	54	DCLKI
55	MODE0	56	MODE1	55	DB_VDD3	56	GND
57	MODE2	58	~RESET	57	DB_VDD3	58	N.C.
59	GND	60	GND	59	DB_VDD3	60	DB_VDDL
61	D0	62	D1	61	SCL	62	SDA
63	D2	64	D3	63	VSYNC	64	HSYNC
65	D4	66	D5	65	CSYNC	66	GV
67	D6	68	D7	67	DE	68	DCLKO
69	DB_VDD3	70	DB_VDD3	69	GND	70	GND
71	D8	72	D9	71	GND	72	GND
73	D10	74	D11	73	GND	74	GND
75	D12	76	D13	75	DV_VPO7	76	DV_VPO6
77	D14	78	D15	77	DV_VPO5	78	DV_VPO4
79	GND	80	GND	79	DV_VPO3	80	DV_VPO2
81	D16	82	D17	81	DV_VPO1	82	DV_VPO0
83	D18	84	D19	83	DV_CCLK	84	DB_VDD3
85	D20	86	D21	85	DB_VDD3	86	DB_VDD3
87	D22	88	D23	87	DB_VDD3	88	DB_VDD3
89	DB_VDD3	90	DB_VDD3	89	N.C.	90	N.C.
91	D24	92	D25	91	VDD5	92	VDD5
93	D26	94	D27	93	N.C.	94	N.C.
95	D28	96	D29	95	GND	96	GND
97	D30	98	D31	97	GND	98	GND
99	GND	100	GND	99	GND	100	GND