

# **MB86291AEB01**

Scarlet[MB86291A] Evaluation System

Hardware Specifications

May 21 2002 (Rev. 1.1 )

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# 1. Overview

This board system is designed to mainly evaluate the functionality and performance of Fujitsu MB86291A "Scarlet" Graphics Display Controller.

This board system can not evaluate "Super Impose Function" using "external sync".

## **2. System Configuration**

### **2.1 Board Configuration**

Depending on the needs, this board can be used either by mounting on a PCI slot of ordinary Windows NT PC or by combining with a specific CPU evaluation board ( A stand alone configuration). The applicable CPU boards are SH-3 EVA BOD(CX06706C-9901, SH3 CPU evaluation board) or SH-4 EVA BOD(CX06710B-9901, SH4 CPU evaluation board) made by Computex, or KZ-V832-01(V832 evaluation board) made by Kyoto Micro Computers, Co. Ltd. When MB86291AEB01 is used with this V832 evaluation board, the dedicated interface adapter board "MB86290EB02" is needed.

When MB86291AEB01 is mounted on a PCI slot, the PCI bus bridge device PCI9054(made by PLX) acts as a local bus master. When MB86291AEB01 is combined with a CPU board, the CPU itself mounted on that board takes this local bus master role.

## 2.2 Component Outline

■ **Scarlet**

MB86291 A(Graphics Display Controller)

■ **PCI bridge**

PCI9054 (made by PLX) and EEPROM [an equivalent 93CS56L]

■ **RGB Encoder MB3516A** (made by Fujitsu)

■ **Digital Video Decoder SAA7113** (made by Philips) and **Bt827** (made by Rockwell)  
(Bt827 is not mounted and Bt827 does not work if you mount it.)

■ **NTSC/PAL Decoder uPC1830** (made by NEC)

■ **Video Sync Separator LM1881** (made by National Semiconductor)

■ **4Fsc Generator EL4584C** (made by Elantec)

■ **8Bit DIP Switch**

Read only

■ **8Bit LED**

Write only

■ **LED**

Power on (Power supply indicator)

■ **CPU Board Interface Connector**

100 pin half pitch x 3

■ **VGA Output Connector**

Dsub15pin female connector

■ **S-VIDEO Input/Output Connector**

Input Connector x1, Output Connector x 1

■ **Composite Video Input/Output Connector**

Input Connector x1, Output Connector x 1

## 2.3 Power Supply

All of the power sources are supplied through interface connectors in either PCI bus mode or Local CPU board combination mode. And this board has power supply connectors which is able to supply the power.

Power connections on this board are as follows,

PCI connector    CPU connector    Power connector

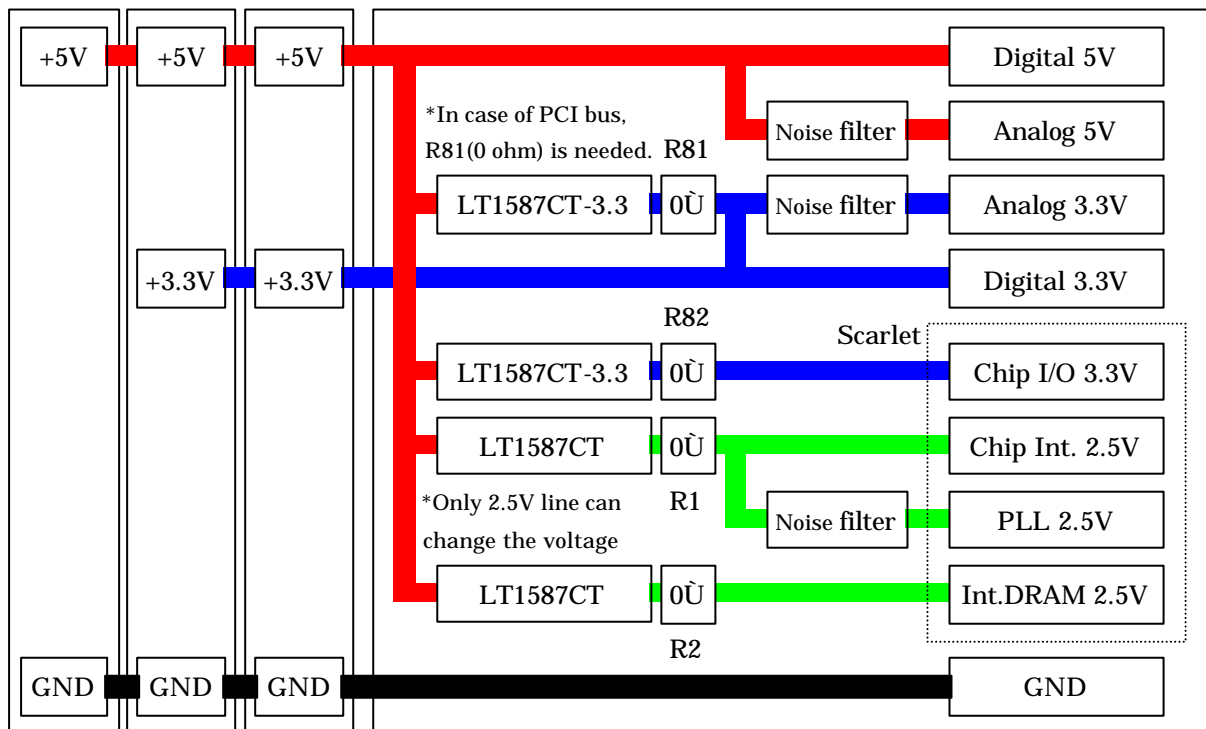


Fig 2-1. MB86291AEB01 Power supply Lines

### 3 Hardware Block Diagram

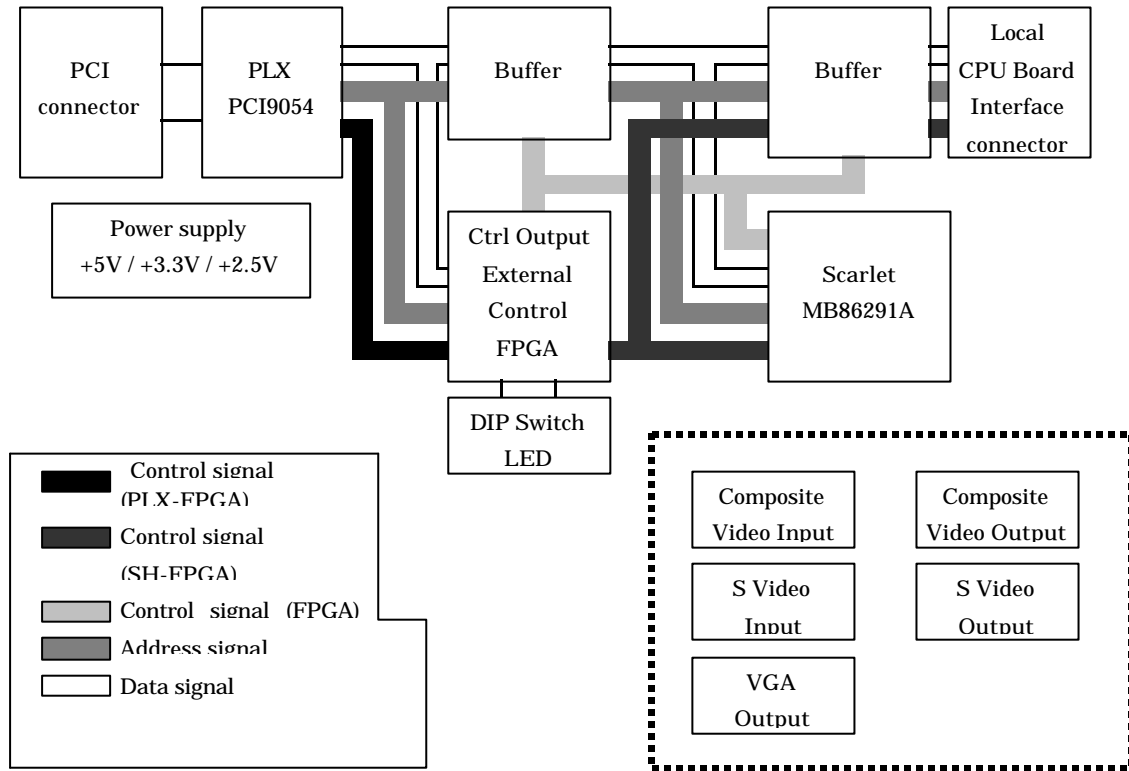


Fig 3-1. MB86291AEB01 Hardware Block Diagram

## 4 Memory Map

### 4.1 Memory Map in PCI bus access mode

1000 0000h	Scarlet		PCI Local Address Space 0
11FB FFFFh	Frame Memory Area	32bit	
11FC 0000h	Scarlet		
11FF FFFFh	Register Area	32bit	
1200 0000h	Scarlet		
13FF FFFFh	Reserved Area	32bit	
1400 0000h	PLX PCI9054		
1400 0FFFh	Internal Register Area	32bit	
1400 1000h	FPGA		
1400 1FFFh	Internal Register Area	32bit	

Table 4-1. MB86291AEB01 Memory Map (PCI bus access mode)

\* MB86291A is embedded only 2MB memory.

## 4.2 Memory Map in Local CPU access mode

1000 0000h	Scarlet		SH_CS4
11FB FFFFh	Frame Memory Area	32bit	
11FC 0000h	Scarlet		
11FF FFFFh	Register Area	32bit	
1200 0000h	Scarlet		SH_CS5
13FF FFFFh	Reserved Area	32bit	
1400 0000h	PLX PCI9054		&A12=0
1400 0FFFh	Internal Register Area	32bit	
1400 1000h	FPGA		SH_CS5
1400 1FFFh	Internal Register Area	32bit	

Table 4-2. MB86291AEB01 memory map (Local CPU access mode)

\* MB86291A is embedded only 2MB memory.

### 4.3 Register Map

Device	Register	Address	Access	Data Size	True State	R/W
LEDR	LED Register	0x1400 1000	32bit	7:0	1=Light	RW
CTLR	Control Register	0x1400 1004	32bit	7:0	1	RW
DIPSWR	DIP Switch Register	0x1400 1008	32bit	7:0	Off=1	RO
OPSWR	Option Switch Register	0x1400 100C	32bit	7:0	Off=1	RO

Table 4-3. MB86291AEB01 Register map

## 4.4 Board Configuration Register

Name :CTRL  
Address :1400 1004H  
Mode Read / Write

Bit	Name	Function	0	1
D4	IMASK	Mask Interrupt (PCI bus access mode )	Disable Scarlet interrupt signal (Default)	Enable Scarlet Interrupt signal
D0	ESE	External sync Enable	Disable	Enable the external Even/Odd signal input to Scarlet in External sync mode

Table 4-4. Board Configuration Register Bit Assignment

## 5 External Appearance

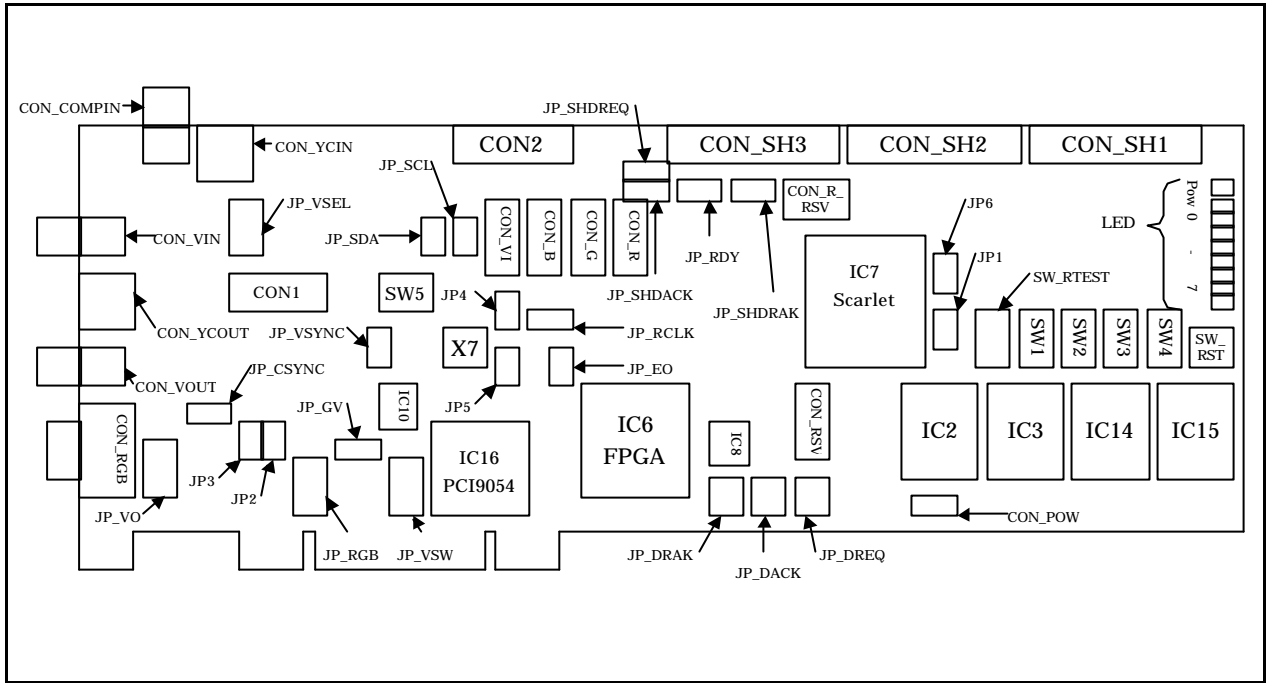


Fig 5-1. MB86291AEB01 External Appearance

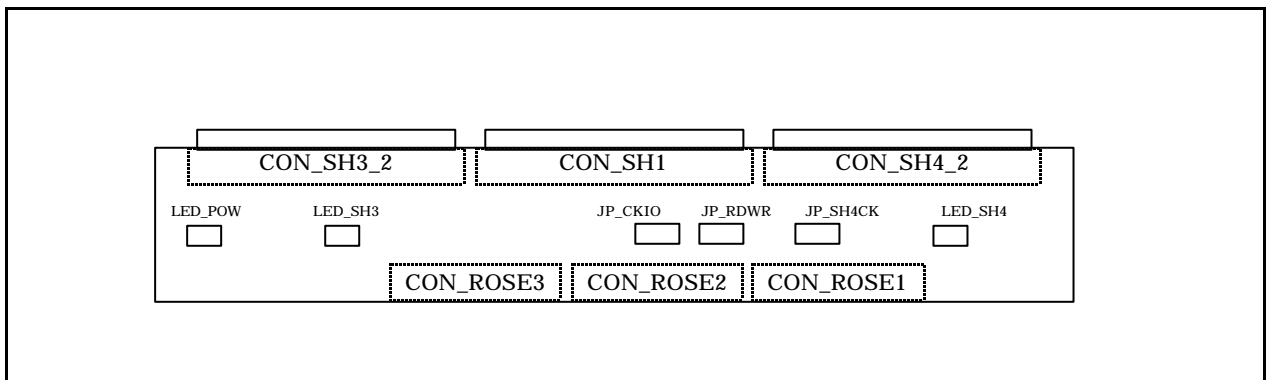


Fig 5-2. Local CPU Connection Board External Appearance

## 5.1 Switch Settings

Switch	Function	Set	Description
SW1-1	PCI9054 TEST signal input	ON	Normal (Default)
		OFF	PCI9054 Test mode
SW1-2	PCI9054 BIGEND# pin input	ON	Local Bus is Big Endian
		OFF	Local Bus is Little Endian (Default)
SW1-3~6	Reserved		
SW1-7	Scarlet (MB86291A) Video I/F External sync clock	ON	2fsc clock
		OFF	4fsc clock(Default)
SW1-8	LVDS interface trigger clock	ON	Negative clock
		OFF	Positive clock (Default)
SW2-1,2	Scarlet (MB86291A) CLKSEL pin input [clock rate of clock mode pin [CKM (SW2-8)=0(ON)]]	Bit1,2	* 1=OFF,0=ON
		0,0	13.5MHz
		0,1	17.73MHz
		1,0	14.32MHz (Default)
		1,1	Reserved
SW2-3,4	Scarlet(MB86291A) Host CPU mode (MODE0,MODE1 pin )	Bit3,4	* 1=OFF,0=ON
		0,0	SH3 mode
		0,1	V832 mode
		1,0	SH4 mode (Default)
		1,1	Reserved
SW2-5	Scarlet (MB86291A) Ready pin mode (MODE2 pin )	ON	Normally Not Ready (Default)
		OFF	Normally Ready
SW2-6	Scarlet (MB86291A) Video I/F EO pin(JP_EO=Open)	ON	EO=L(Even Field)
		OFF	EO=H(Odd Field) (Default)
SW2-7	Scarlet(MB86291A) OSCCNT pin	ON	Exhibit to set (Low level input)
		OFF	High level input (Default)
SW2-8	Scarlet (MB86291A) Set Clock Mode(CKM pin)	ON	Scarlet Internal PLL Output(Default)
		OFF	Host CPUBus Clock(BCLKI)
SW3-1	Scarlet (MB86291A) PLL Reset signal(S pin)	ON	Low level input
		OFF	High level input (default)
SW3-2	Board Connector settings	ON	Local CPU bus connection mode
		OFF	PCI bus connection mode(Default)
SW3-3~8	Reserved		
SW4-1~8	DIP Switch	ON=0 OFF=1	Bit1=LSB Bit8=MSB (Default All OFF)

Table 5-1. MB86291AEB01 Switch settings (1)

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Switch	Function	Set	Description
SW5-1	GV Signal( RGB switch) setting (in case of set JP_GV to 1-2, it is available.	ON	GV=L(Select Video output )
		OFF	GV=H(Select Scarlet output) (Default)
SW5-2,3	Reserved		
SW5-4	EL4584C PROGA pin input		OFF=High ON=Low(Default:OFF)
SW5-5	EL4584C PROGB pin input		OFF=High ON=Low(Default:OFF)
SW5-6	EL4584C PROGC pin input		OFF=High ON=Low(Default:OFF)
SW5-7	EL4584C DIVSEL pin input		OFF=High ON=Low(Default:OFF)
SW5-8	EL4584C COAST pin input		OFF=High ON=Low(Default:OFF)
SW_RTEST -1~6	Scarlet (MB86291A) TESTH pin input	ON	Input Low
		OFF	Input High (Default)
SW_RTEST -7,8	Scarlet (MB86291A) TESTL pin input	ON	Input Low (Default)
		OFF	Input High
SW_RST	RESET pin input		

table5-2. MB86291AEB01 Switch settings (2)

## 5.2 Jumper settings

### 5.2.1 Jumper settings of MB86291AEB01

Jumper	Function	Set	Description
JP_VSW	Scarlet Output RGB signal connection (1)	Short	Input to RGB switch and connect 75 ohm terminator
		Open	Not input to RGB switch and no 75 ohm terminator is connected
JP_RGB	Scarlet Output RGB signal connection (2)	1-2	Connect RGB output of Scarlet to MB3516(RGB Encoder)
		2-3	Connect RGB switch output to MB3516(RGB Encoder) (Default)
JP_VO	Scarlet Output RGB signal connection (3)	1-2	Connect RGB output of Scarlet to VGA connector directly(Default)
		2-3	Connect output signal of MB3516 to VGA connector
JP_VSEL	Selection of Video Decoder	1-2	Use SAA7113 (Default)
		2-3	Use Bt829(Not mounted)
JP_EO	Scarlet Video I/F EO pin setting	Short	Use EVEN/ODD output of LM1881(Sync Separator) (Default)
		Open	SW2-6 is valid (Refer SW2-6 section)
JP_VSYNC	Selection of VSYNC input to Scarlet	1-2	Use VSYNC output of LM1881 (Default)
		2-3	Use VSYNC output of uPC1830
JP_CSYNC	Selection of CSYNC input to MB3516	1-2	Use CSYNC output of Scarlet (Default)
		2-3	Use CSYNC output of LM1881
JP_GV	Selection of Control signal of NJM2286(RGB Switch)	1-2	SW5-1 is valid (Refer SW5-1 section)
		2-3	Connect GV output of Scarlet (Default)
JP_RCLK	Scarlet Bus clock input	1-2	Positive clock (Default)
		2-3	Negative clock
JP-RDY	Scarlet RDY signal Pull-Up/Pull-Down	1-2	RDY signal is Pull-Up
		2-3	RDY signal is Pull-Down
		Open	No Pull-Up/Pull-Down (Default)
JP_SCL	I2C I/F SCL signal input	1-2	SCL signal connect to Scarlet output
		2-3	SCL signal connect to FPGA output (Default)
JP_SDA	I2C I/F SDA signal input	1-2	SDA signal connect to Scarlet output
		2-3	SDA signal connect to FPGA output (Default)

Table 5-3. MB86291AEB01 Jumper Settings (1)

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Jumper	Function	Set	Description
JP_SHDACK	Local CPU board I/F DACK signal	1-2	DACK0 signal is used
		2-3	DACK1 signal is used (Default)
JP_SHDRAK	Local CPU board I/F DRAK signal	1-2	DRAK0 signal is used
		2-3	DRAK1 signal is used (Default)
JP_SHDREQ	Local CPU board I/F DREQ signal	1-2	DREQ0 signal is used
		2-3	DREQ1 signal is used (Default)
JP_DACK	Local CPU board I/F DTACK signal	2-4	Fixed (Default)
JP_DRAK	Local CPU board I/F DRACK signal	2-4	Fixed (Default)
JP_DREQ	Local CPU board I/F DREQ signal	2-4	Fixed (Default)
JP1,JP6	Scarlet CLK signal input	JP1:1-2,JP6:Open	X8 input (Default)
		JP1:2-3,JP6:Short	X1 input
		Other settings	Exhibit
JP2	MB3516 FSC clock input	1-2	Connect X-Tal output (3.579545MHz) (Default)
		2-3	Connect DCLKO output of Scarlet
JP3	MB3516 NTSC/PAL mode	1-2	NTSC mode(Default)
		2-3	PAL mode
JP4,JP5	Bus clock signal mode	JP4:1-2 JP5:Don't Care	Local CPU board mode
		JP4:2-3 JP5:1-2	PCI bus mode X7 is used (Default)
		JP4:2-3 JP5:2-3	PCI bus mode Scarlet CCLK is used
		Others	Reserved

Table 5-4. MB86291AEB01 Jumper Settings (2)

## 5.2.2 Jumper Settings of Local CPU Connection Board

Jumper	Function	Set	Description
JP_CKIO	Local CPU board Bus clock	1-2	SH3 board is connected
		2-3	SH4 board is connected (Default)
JP_RDWR	Local CPU board RDWR signal	1-2	SH3 board is connected
		2-3	SH4 board is connected (Default)
JP_SH4CK	SH4 I/F	1-2	CKIO1 is used (Default)
	Local Bus clock	2-3	CKIO2 is used

Table 5-5. Local CPU Connection Board Jumper Settings

## 5.2.3 Switch and Jumper Settings

### 5.2.3.1 Change PCI bus mode or Local CPU board mode

The switch and jumper settings for PCI bus mode or Local CPU board mode are follows:

Default is set to PCI bus mode.

In case of PCI bus mode, CPU mode(SW2-3,4) has to be set to SH4 mode, Ready mode(SW2-5) has to be set to "Normally Not Ready" mode.

Mode	SW1-1	SW2-3,4	SW2-5	SW3-2	JP4
PCI bus mode	ON	OFF,ON(SH4 mode)	ON	OFF	2-3
Local CPU board mode	OFF	Depend on CPU	OFF	ON	1-2

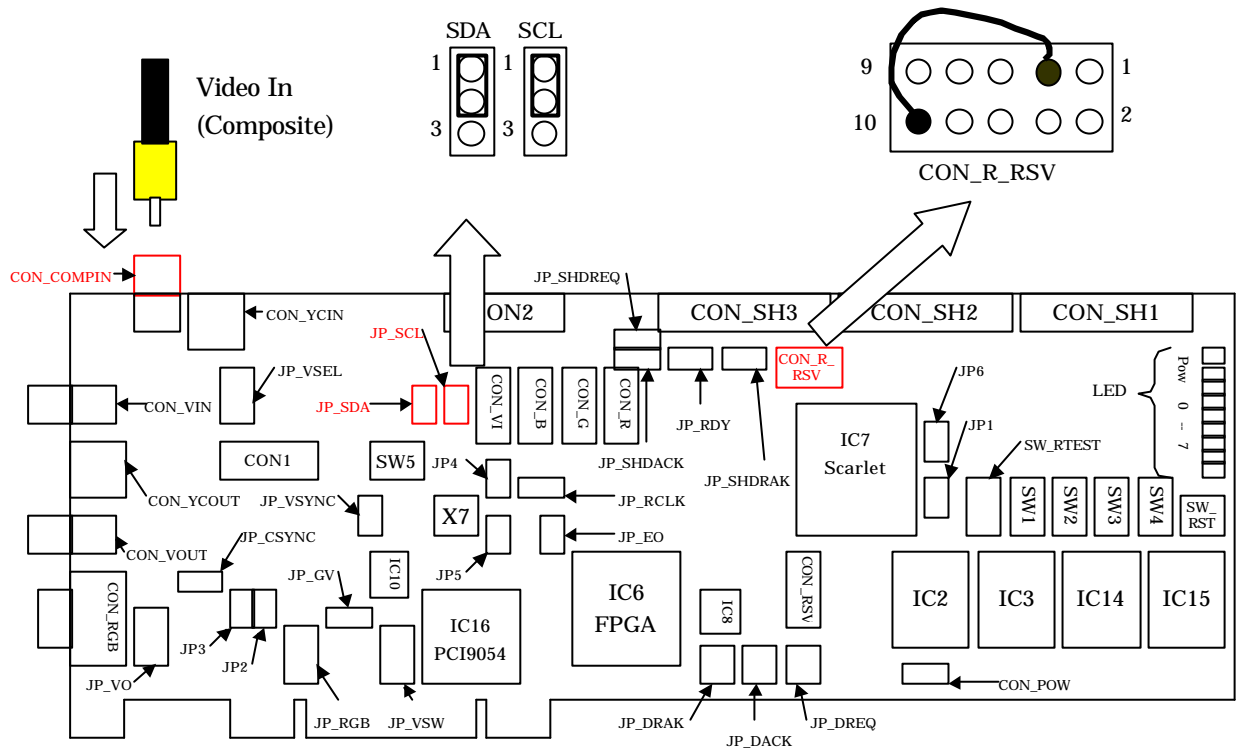
### 5.2.3.2 Jumper setting for Video Capture

In case of evaluating video capture function, please set jumpers as follows.

JP\_SDA : 1-2

JP\_SCL : 1-2

CON\_R\_RSV : Connect Pin3 and Pin10 by wire.



## 5.3 Switch and Jumper Settings of Video Output Control Block

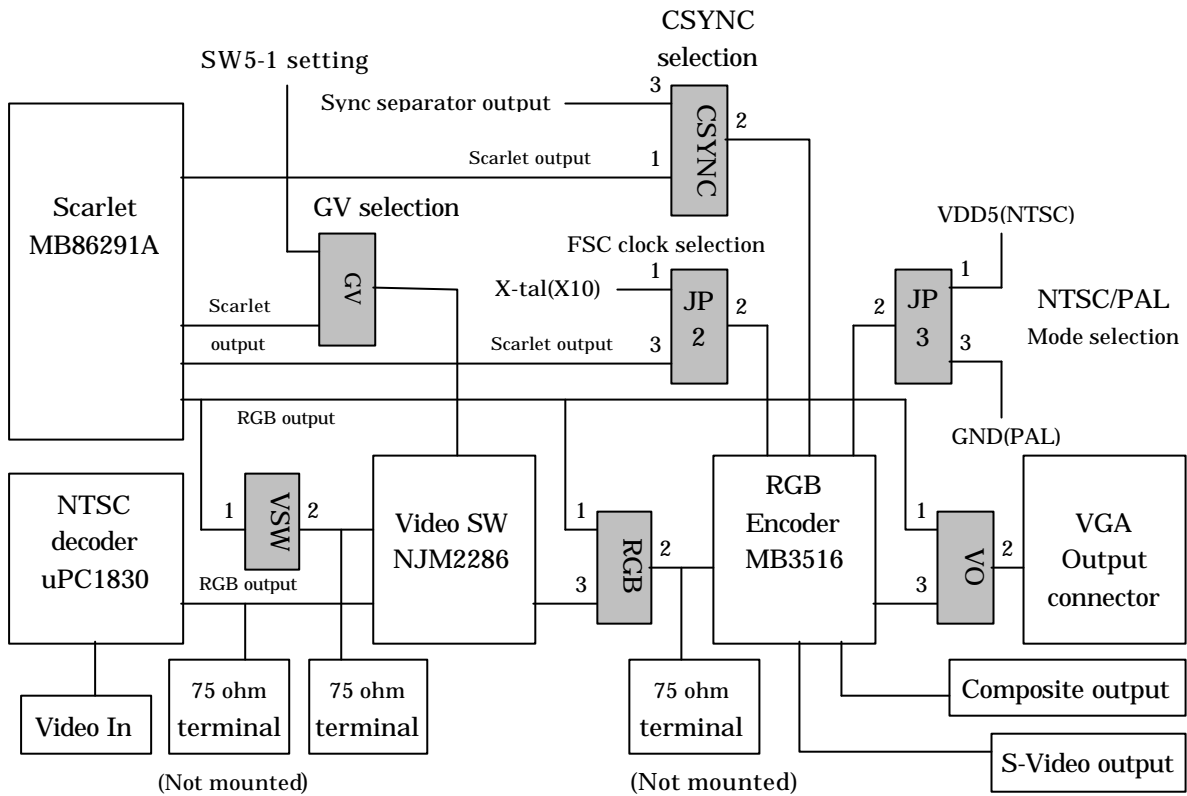


Fig 5-3. MB86291AEB01 Video Control Block Diagram

Setting	VSW	RGB	VO	CSYNC	JP2	GV	JP3
RGB output from Scarlet is directly connected to VGA connector	Short:*1 Open:*2	2-3 (Don't care)	1-2	Don't care	Don't care	Don't care	Don't care
VIDEO SW output is connected to each output connector (VGA/Composite/S Video)	Short	2-3	2-3	1-2	1-2	2-3	Don't care

\*1: With 75 ohm terminal

\*2: Without 75 ohm terminal

Table 5-6. MB86291EB01 Switch and Jumper setting table for Video output control block

## 5.4 MB86291AEB01 Connector for Local CPU Interface Board

This board has three special connectors to interface to local CPU board (SH3:SH7709A and SH4:SH7750 are the expected host CPU for this board).

Using Local CPU Connection Board that is temped with MB86291AEB01, MB86291AEB01 is able to connect directly with Local CPU board.

Note) **The interrupt signal from Scarlet is connected to IRL2 and IRL3 signal of SH connector through FPGA.**

Status of Scarlet Interrupt signal	Status of IRL[3:0] in SH connector
Low(Interrupt)	0x3
High(No Interrupt)	0xf

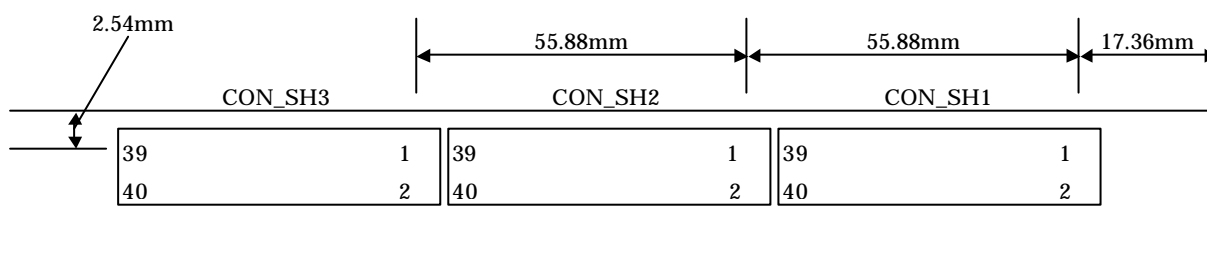


Fig 5-4. Install position of MB86291EB01 board for Local CPU interface connector

<Using connector (CON\_SH1~CON\_SH3)>

Pin pitch 2.54mm, 2Lines x 20pin header

<Part Number of these connector>

PS-40SD-D4TS1-1 (made by JAE)

## Signal Pin Assignment for Local CPU Interface board

CON_SH1				CON_SH2			
1	~CS0	2	~WE0	1	VDD5	2	VDD3
3	~CS1	4	~WE1	3	A2	4	A3
5	~CS2	6	~WE2	5	A4	6	A5
7	~CS3	8	~WE3	7	A6	8	A7
9	VDD5	10	VDD3	9	VDD5	10	VDD3
11	~CS4	12	RDWR	11	A8	12	A9
13	~CS5	14	~BS	13	A10	14	A11
15	~CS6	16	GND	15	A12	16	A13
17	~RD	18	CKIO	17	A14	18	A15
19	GND	20	GND	19	GND	20	GND
21	~IRL0	22	~IRL1	21	A16	22	A17
23	~IRL2	24	~IRL3	23	A18	24	A19
25	~RESETOUT	26	RDY	25	A20	26	A21
27	~BACK	28	~BREQ	27	A22	28	A23
29	VDD5	30	VDD3	29	VDD5	30	VDD3
31	DRAK1	32	DRAK0	31	A24	32	A25
33	~DREQ0	34	DACK0	33	VDD5	34	VDD3
35	~DREQ1	36	DACK1	35	GND	36	GND
37	GND	38	GND	37	GND	38	GND
39	GND	40	GND	39	GND	40	GND

CON_SH3			
1	D0	2	D1
3	D2	4	D3
5	D4	6	D5
7	D6	8	D7
9	VDD5	10	VDD3
11	D8	12	D9
13	D10	14	D11
15	D12	16	D13
17	D14	18	D15
19	GND	20	GND
21	D16	22	D17
23	D18	24	D19
25	D20	26	D21
27	D22	28	D23
29	VDD5	30	VDD3
31	D24	32	D25
33	D26	34	D27
35	D28	36	D29
37	D30	38	D31
39	GND	40	GND

Table 5-7. Connectors pin assignment for Local CPU Interface board

## 5.5 Local CPU Interface Board

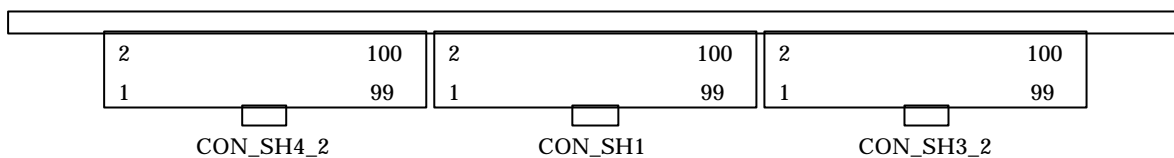


Fig5-5. Top view of Local CPU Interface Board

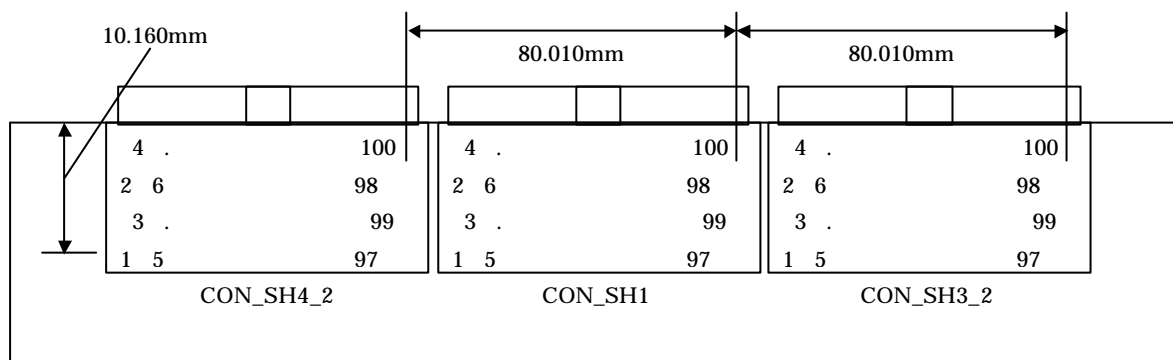


Fig5-6. Install position of Local CPU interface board

<Part number of these connector(CON\_SH1,CON\_SH3\_2,CON\_SH4\_2)>  
 TX14-100R-LT-MH1 (made by JAE)

<Part number of connected side connector(SH board side)>  
 TX15-100P-LT-MH1 (made by JAE)

## Signal Pin Assignment of Local CPU Interface Board

CON_SH4_2(SH4 Connect only)				CON_SH3_2(SH3 Connect only)			
1	GND	2	GND	1	GND	2	GND
3	GND	4	GND	3	GND	4	GND
5	VDD3	6	VDD3	5	VDD3	6	VDD3
7	VDD3	8	VDD3	7	VDD3	8	VDD3
9	N.C.	10	N.C.	9	SH3_CKIO	10	N.C.
11	N.C.	12	N.C.	11	N.C.	12	N.C.
13	N.C.	14	N.C.	13	SH_WAIT	14	N.C.
15	N.C.	16	N.C.	15	~SH_BACK	16	~SH_BREQ
17	N.C.	18	N.C.	17	N.C.	18	N.C.
19	N.C.	20	N.C.	19	N.C.	20	N.C.
21	N.C.	22	N.C.	21	N.C.	22	N.C.
23	N.C.	24	N.C.	23	N.C.	24	N.C.
25	N.C.	26	N.C.	25	N.C.	26	N.C.
27	N.C.	28	N.C.	27	N.C.	28	N.C.
29	N.C.	30	N.C.	29	DRAK1	30	DRAK0
31	N.C.	32	N.C.	31	~RESETOUT	32	N.C.
33	N.C.	34	N.C.	33	~DREQ0	34	DACK0
35	N.C.	36	N.C.	35	~DREQ1	36	DACK1
37	N.C.	38	N.C.	37	N.C.	38	N.C.
39	N.C.	40	N.C.	39	N.C.	40	N.C.
41	GND	42	GND	41	GND	42	GND
43	N.C.	44	N.C.	43	N.C.	44	N.C.
45	N.C.	46	N.C.	45	N.C.	46	N.C.
47	N.C.	48	N.C.	47	N.C.	48	N.C.
49	N.C.	50	N.C.	49	N.C.	50	N.C.
51	~SH_IRL0	52	~SH_IRL1	51	N.C.	52	N.C.
53	~SH_IRL2	54	~SH_IRL3	53	N.C.	54	N.C.
55	~DREQ0	56	~DREQ1	55	N.C.	56	N.C.
57	DRAK0	58	DRAK1	57	N.C.	58	N.C.
59	DACK0	60	DACK1	59	N.C.	60	N.C.
61	~CKIO2ENB (GND)	62	N.C.	61	N.C.	62	N.C.
63	SH4_RDWR	64	N.C.	63	~SH_IRL0	64	~SH_IRL1
65	N.C.	66	N.C.	65	~SH_IRL2	66	~SH_IRL3
67	N.C.	68	~SH_BS	67	N.C.	68	N.C.
69	SH_BACK	70	~SH_BREQ	69	N.C.	70	N.C.
71	N.C.	72	N.C.	71	N.C.	72	N.C.
73	N.C.	74	SH_WAIT	73	N.C.	74	N.C.
75	N.C.	76	N.C.	75	N.C.	76	N.C.
77	N.C.	78	N.C.	77	N.C.	78	N.C.
79	CKIO2	80	N.C.	79	~SH_BS	80	N.C.
81	N.C.	82	N.C.	81	N.C.	82	N.C.
83	CKIO1	84	N.C.	83	N.C.	84	N.C.
85	N.C.	86	N.C.	85	N.C.	86	N.C.
87	~RESETOUT	88	N.C.	87	N.C.	88	N.C.
89	N.C.	90	N.C.	89	N.C.	90	N.C.
91	N.C.	92	N.C.	91	N.C.	92	N.C.
93	VDD3	94	VDD3	93	VDD3	94	VDD3
95	VDD3	96	VDD3	95	VDD3	96	VDD3
97	GND	98	GND	97	GND	98	GND
99	GND	100	GND	99	GND	100	GND

Table 5-8. Signal Pin Assignment of Local CPU Interface board (1)  
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CON_SH1(SH3 & SH4 Connect)			
1	GND	2	GND
3	GND	4	GND
5	VDD5	6	VDD5
7	VDD5	8	VDD5
9	A0*	10	A1*
11	SH_A2	12	SH_A3
13	SH_A4	14	SH_A5
15	SH_A6	16	SH_A7
17	SH_A8	18	SH_A9
19	SH_A10	20	SH_A11
21	SH_A12	22	SH_A13
23	SH_A14	24	SH_A15
25	SH_A16	26	SH_A17
27	SH_A18	28	SH_A19
29	SH_A20	30	SH_A21
31	SH_A22	32	SH_A23
33	SH_A24	34	SH_A25
35	N.C.	36	N.C.
37	N.C.	38	N.C.
39	N.C.	40	N.C.
41	GND	42	GND
43	SH_D0	44	SH_D1
45	SH_D2	46	SH_D3
47	SH_D4	48	SH_D5
49	SH_D6	50	SH_D7
51	SH_D8	52	SH_D9
53	SH_D10	54	SH_D11
55	SH_D12	56	SH_D13
57	SH_D14	58	SH_D15
59	SH_D16	60	SH_D17
61	SH_D18	62	SH_D19
63	SH_D20	64	SH_D21
65	SH_D22	66	SH_D23
67	SH_D24	68	SH_D25
69	SH_D26	70	SH_D27
71	SH_D28	72	SH_D29
73	SH_D30	74	SH_D31
75	~SH_CS0	76	~SH_WE0
77	~SH_CS1	78	~SH_WE1
79	~SH_CS2	80	~SH_WE2
81	~SH_CS3	82	~SH_WE3
83	~SH_CS4	84	N.C.
85	~SH_CS5	86	N.C.
87	~SH_CS6	88	N.C.
89	N.C.	90	N.C.
91	~SH_RD	92	SH3_RDWR
93	VDD5	94	VDD5
95	VDD5	96	VDD5
97	GND	98	GND
99	GND	100	GND

\*A0 and A1 are not used in this board

Table5-9. Signal Pin Assignment of Local CPU Interface board (2)