

GRAPHICS CONTROLLERS

MB88F332 'INDIGO'

APIX[®] PIXELLINK SYNCHRONIZATION

APPLICATION NOTE

**GRAPHICS COMPETENCE
CENTER**



Revision History

Date	Issue
2009-06-09	Rev 0.01 GCC/HA First draft
2009-06-16	Rev 0.02 GCC/HA Review and minor corrections
2009-07-28	Rev 0.5 GCC/HA Used new template – review by HW Group, more detailed explanation
2009-07-29	Rev 0.6 GCC/HA Document formatting

This document contains 15 pages.

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1 Introduction

This document describes the needed steps for setting up and configuring the Fujitsu GDC MB88F332 (short name in this document 'Indigo') for using it together with a video stream fed into the system via APIX[®] pixellink. The video stream data is usually coming from an external device with either an integrated APIX[®] transmitter (like Fujitsu's MB86R02 'Jade-D') or is generated independently and transmitted via a discrete APIX[®] TX transmitter. The focus of this application note is not the settings of the APIX[®] physical layer nor the proper configuration of the APIX[®] link itself.

It focuses on the parameters that are relevant and need to be adjusted to have a reliable transmission of the video stream data. A suitable configuration of the panel parameters and timings for the video display controller and/or the timing controller is discussed as well. Additionally the mechanics of the complete transmission line from the source via the link to the target are explained.

2 Prerequisites

To set up a working system for a video data transmission via the APIX[®] pixellink several constraints have to be fulfilled. The most important ones are:

2.1 PHY Level

The physical APIX[®] layer setting has to match the requirements of the video data stream like bandwidth, colour depth etc. For details please refer to the indigo hardware manual, chapter 5 (APIX[®] Interface) and chapter 6 (Remote Handler). Please follow this link for the latest version:

<http://www.fujitsu.com/emea/services/microelectronics/gdc/gdcdevices/mb88f332-indigo.html>

2.2 Video data TX and RX matching

The video parameters (like resolution etc.) on the generator side have to fit to the settings on the target (Indigo) side. A deviation of several parameters is possible but certain restrictions have to be fulfilled. Details and examples will be given later in this document.

2.3 Display Panel Hardware

The attached panel on the Indigo side needs to match the requirements of the video data stream as well. In general scaling of video is not supported by Indigo. Also a transmission of a smaller video resolution to a bigger panel (e.g. 640*480 video stream to a 800*600 panel) may work or not. This depends entirely on the panel specification and would leave some areas of the panel unused (in case that the specification of the panel supports this). Transmitting a bigger stream to a smaller panel is also panel specific, too. The overhead of pixels that can't be displayed would be discarded, but maybe with visible artifacts.

For proper operation it is strongly recommended to use only matching size of video data and panel resolution.

3 The Video Data Generator and Transmitter side

3.1 Example

Assuming the video data signal is generated by Fujitsu's Jade or Jade-D device. A possible setup would use a timing like this (panel size is 800 * 480 active area):

HTP	=	1056
HSP	=	840
HSW	=	128
HDP	=	800
VTR	=	569
VSP	=	491
VSW	=	2
VDP	=	480

At a given 60 Hz panel frame rate frequency this will result in a pixelclock of approximately 36 MHz on the transmitter side. For details please see the figure below.



HTP	Horizontal Total Pixels	VTR	Vertical Total Raster
HSP	Horizontal Synchronize pulse Position	VSP	Vertical Synchronize pulse Position
HSW	Horizontal Synchronize pulse Width	VSW	Vertical Synchronize pulse Width
HDP	Horizontal Display Period	VDP	Vertical Display Period

Figure 3-1 Panel parameters and explanation of main abbreviations

4 The Receiver Side MB88F332 Indigo

Please adjust the settings for the video display controller according to the given settings of the transmitter and make sure that the panel specification is not violated. Refer to chapter 9 (Video Display Controller) in Indigo's hardware manual for further details about the register settings.

Due to the granularity of Indigo's clock system please choose a Bitclock (= pixelclock *2) as near as possible to the transmitter wise selected pixelclock. Refer to the chapter 19 (Clock and Reset Generator) and there to the section "Clksynth" for more details.

Depending on the panel type (TTL or RSDS) please configure the TCON unit of Indigo according to the panel specification.

When using the integrated TCON module of Indigo please have in mind that the settings for the Video Display Controller will be used as the "Master settings" within the system. The settings and values used in the TCON module reference to these values. Please refer to chapter 10 (Timing Controller), section "Coordinate space", for further explanation of the dependencies between the two modules.

5 The System Setup

5.1 System start and verification

After successfully starting up the system the “ASStatus” register in Indigo (Chapter 6, Remote handler) should indicate at least at the status bit 1 “rx_pll_good” = “1” and bit 7 “rx_px_aligned” = “1” as soon as the transmitter starts sending the video data. Additionally the “operational” = “1” (bit 2) would indicate that the sideband data is used additionally to the video data.

Status bits like fatal_error, rx_crc_error, crc_timeout, protocol_error (bits 0,3,6,8) and increasing counters like rx_crc_error_cnt and sync_loss_cnt (please check the corresponding registers in the remote handler section of the hardware manual) would indicate that the APIX[®] link is not running reliably. In this case please make sure that the link is running properly by checking the settings again and also verifying the hardware. Another application note covering the layout topic is available via this link as well: [Application Note \(APIX Layout Recommendations\)](#).

When running the system without a stable connection side effects can arise that will be hard to identify later on and slow down the integration process.

5.2 The Pixellink

The APIX[®] link is divided into two separate logical paths. To control the Indigo a so call side-band channel is used. This enables the user to manipulate the registers of the MB88F332. Independently the video stream data is send with much higher bandwidth via the so called Pixellink. This videolink itself consists internally of up to 24 bit pixel information and 3 control signals for Hsync, Vsync and DE (display enable). These (in total up to) 27 pins would be connected to the discrete IC from Inova when a separate video source should be used. If an integrated solution is used (transmitter is integrated in the IC like e.g. in Fujitsu’s Jade-D) these internal signals are connected to the internal APIX[®] physical layer logic.

On the indigo side then the up to 24 bit pixel data are taken directly to the display controller. The pixel control data signals are handled by the display controller as well (see figure 5-1, next page).

One task of the Video Display Controller is the synchronization of the external video timing with the Indigo internal video timing for every line. The Indigo internal line frequency is aligned to external line frequency by adjusting the number of cycles during the horizontal front porch. See description of the “External Horizontal Display Parameter State Machine” within chapter 9 of the HW manual. Another task is to handle pixelclock differencies between video source and Indigo. In the Video Display Controller module the video pixel data (up to 24 bit “native” pixel data) is fed into the so called PixelFiFo. The registers “PFC” - including an adjustable horizontal delay (HDELAY) - and “PFD” including PixelFiFoDepth (PDMIN/PDMAX) inform about the PixelFiFo status. Please refer to chapter 9 and there to the register description for details.

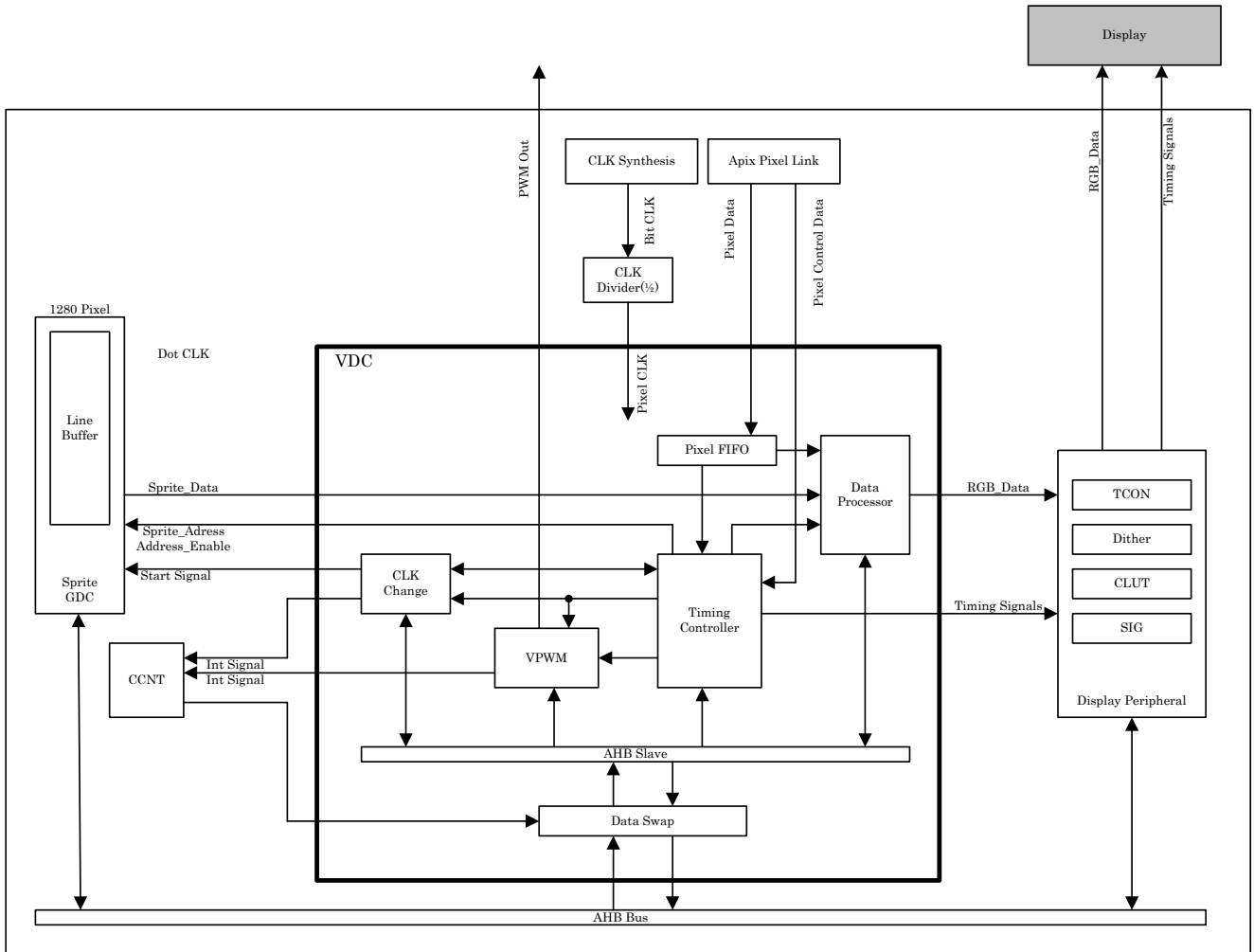


Figure 5-1 VDC and APiX[®] Pixellink

5.3 The different clock speeds

First goal is to match the refresh rate of the panel attached to the MB88F332 (and therefore the pixelclock) to the transmitting side. Please select the best matching clock dividers. In case that the Indigo pixel clock can not be fine tuned via the “Nominal Frequency” register in the “Clock Synthesis” module (please see chapter 19, “clock and reset generator”) with the parameters Ndiv, Pdiv and Psub it is maybe necessary to adjust the HTP and VTR in accordance to the panel specification.

The delay (HDELAY) in the PixelFifo can additionally be used to compensate different speeds between transmitter and receiver PixelFifo. The basic estimate for the deviation is calculated like this:

Maximum PixelFifo depth is 128 pixel. Assuming the active horizontal pixels in this example is 800 pixel the PixelFifo would cover approx. 15% of the data per line. The PixelFifo handles the active pixels only, the control signals are not taken into account. This implies that in principle a clock difference between transmitter and receiver of up to 15% could be covered. To have a coverage that is uniformly distributed you need to divide the value by 2 so that 7,5 % can be handled. Please consider that the actual values are less because of additional internal synchronisation processes.

One constraint at this point is again that the panel specification needs to allow to modify the HTP and VTR accordingly to run at the defined refresh rate if the deviation of both pixelclocks gets to big.

In case that the transmitter (HU) pixelclock is running faster than the receiver (Indigo) the delay in the PixelFifo should be set to a low level so that the buffer can catch up the incoming data ($fCLK_{HU} > fCLK_{Indigo}$). Please see figure 5-2 for a schematic overview.

The opposite case ($fCLK_{HU} < fCLK_{Indigo}$) can be adjusted by setting the delay to a higher value to allow the buffer to be filled up first before the faster indigo starts to read out data (figure 5-3).

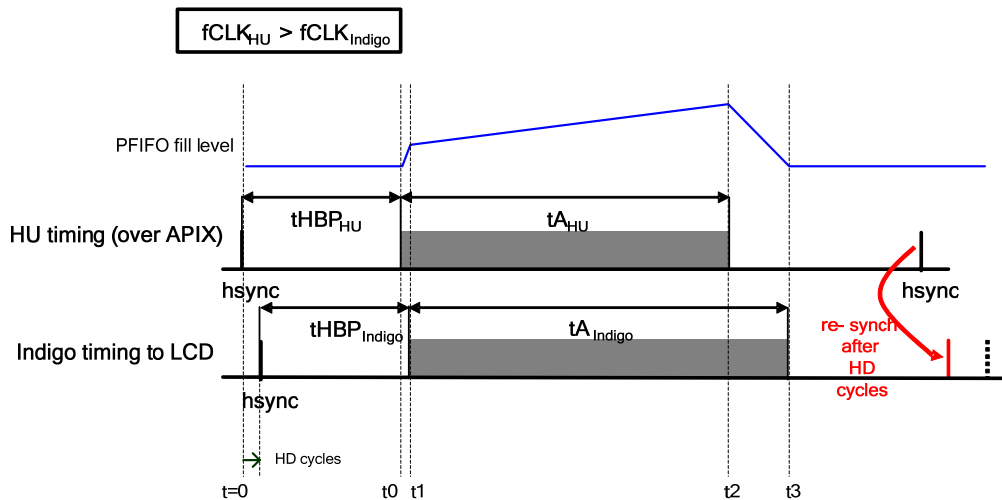


Figure 5-2 Relation of PixelFifo level and different clockspeeds (1/2)

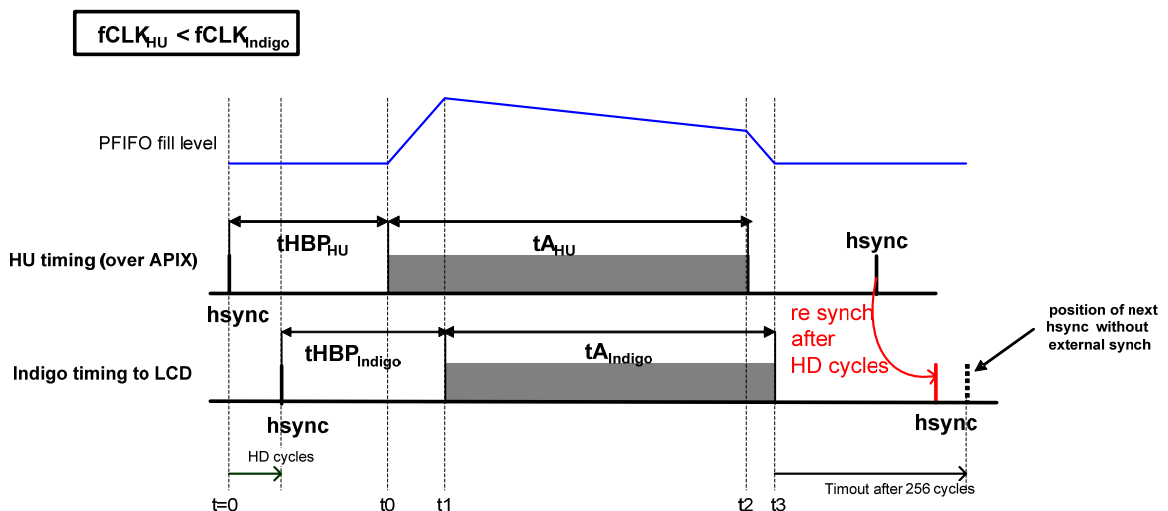


Figure 5-3 Relation of PixelFifo level and different clockspeeds (2/2)

The PDMAX register should float around a given value in steps of a few pixels. This is the normal behavior. If you observe a fixed value (usually 0 or bigger than 128) please check again the settings for the panel in the video display controller module because this gives an indication that the TX and RX parameters are not matching. Additionally you will observe a PixelFiFo under- or overflow interrupt/error as well.

Please note that the “HDELAY” value needs to take into account additional capacity for buffering external impacts like e.g. temperature drifts of several parameters. This means the buffer needs to have some additional headroom calculated. This further decreases the estimate of the 7.5% in our example.

5.4 The Synchronization

The control signals transmitted via the APIX[®] pixellink are used to synchronize the data coming from the sprite engine and the VDC together with the data coming from the video stream within the pixellink. In case that one of the Hsync signals coming from the transmitter side is missing or disturbed the external synchronization is lost. Nevertheless Indigo’s internal synchronisation is running and will generate this signal after reaching a given timeout value (dot line in figures 5-3, marked as “timeout after 256 cycles”).

To run the pixellink successfully please obey to the rules and formulae described in chapter 6 “Rules to observe” on the next page. This is mandatory for proper operation. The summary is derived from the document as a wrap up and additionally covers internal constraints in indigo as well (e.g. some registers have minimal default settings).

6 Rules to observe

- [1] External horizontal sync signal (HSYNC_{hu}) must not arrive at Indigo display controller module during active pixel time of Indigo (HDP_{ind})

$$HSP_{ind} > HDP + HTP_{ind} - HTP_{hu} \cdot \frac{f_{ind}}{f_{hu}} + m$$

m = margin = 4 cycles (reason APIX[®] jitter, Indigo quartz accuracy)

- [2] Indigo requirement: HFP_{ind} < 255 cycles (Time out for external HSYNC)

$$HSP_{ind} < 255 + HDP + HTP_{ind} - HTP_{hu} \cdot \frac{f_{ind}}{f_{hu}} - m$$

m = margin = 4 cycles (reason APIX[®] jitter, Indigo quartz accuracy)

- [3] Avoid over- and underflow of Indigo active pixel FIFO

for $f_{ind} > f_{hu}$:

$$HD < (128 - m + HTP_{hu} - HSP_{hu}) \cdot \frac{f_{ind}}{f_{hu}} - HTP_{ind} + HSP_{ind}$$

$$HD > (HTP_{hu} - HSP_{hu} + HDP) \cdot \frac{f_{ind}}{f_{hu}} + m - HTP_{ind} + HSP_{ind} - HDP$$

$f_{hu} > f_{ind}$:

$$HD < (HTP_{hu} - HSP_{hu} + HDP) \cdot \frac{f_{ind}}{f_{hu}} + 128 - m - HTP_{ind} + HSP_{ind} - HDP$$

$$HD > (HTP_{hu} - HSP_{hu}) \cdot \frac{f_{ind}}{f_{hu}} - HTP_{ind} + HSP_{ind} + m$$

- [4] Vertical Alignment, please observe

$$VTR_{ind} = VTR_{hu}$$

$$VSP_{ind} = VSP_{hu}$$

$$VTR_{ind} - VSP_{ind} = VTR_{hu} - VSP_{hu}$$

$$VDP_{ind} = VDP_{hu}$$

[5] Indigo requirements, see also Indigo hardware manual:

- a. $0 < HDP_{ind} < HSP_{ind} < HSP_{ind} + HSW_{ind} < HTP_{ind}$
- b. $0 < VDP_{ind} < VSP_{ind} < VSP_{ind} + VSW_{ind} < VTR_{ind}$
- c. $HSW_{ind} > 3$
- d. $VSW_{ind} > 1$
- e. $HTP_{ind} > 31$
- f. $VTR_{ind} > 31$
- g. $HDP_{ind} > 15$
- h. $HSP_{ind} > 19$

[6] APIX[®] bandwidth requirement for 18 bit per pixel ($f_{hu} < 42\text{MHz}$)

[7] Do not violate requirements of panel specification, especially the column and row driver specifications. For the generation of column and row driver control pulses please use the Indigo TCON module. Please be aware that the coordinate system of the TCON module is relative to the Indigo display controller module's HSync position. The duration of Indigo's display controller module's HFP period is therefore not constant.

[8] Choose optimum HSP_{ind} to allow maximum f_{hu} variance

$$HSP_{ind, opt} = 128 + HDP + HTP_{ind} - HTP_{hu} \cdot \frac{f_{ind}}{f_{hu}}$$

[9] Choose optimum HD to allow maximum f_{hu} variance

$$HD_{opt} = \frac{f_{ind}}{f_{ind} + f_{hu}} \cdot (128 + HTP_{hu} + HTP_{ind} - HSP_{hu} - HSP_{ind} + HDP + (HTP_{hu} - HSP_{hu} + HDP) \cdot \frac{f_{ind}}{f_{hu}} - (HTP_{ind} + HSP_{ind}) \cdot \frac{f_{hu}}{f_{ind}})$$

7 Abbreviations

HTP	Horizontal Total Pixels
HSP	Horizontal Synchronize pulse Position
HSW	Horizontal Synchronize pulse Width
HDP	Horizontal Display Period
VTR	Vertical Total Raster
VSP	Vertical Synchronize pulse Position
VSW	Vertical Synchronize pulse Width
VDP	Vertical Display Period
Hsync	Horizontal Synchronisation Signal
Vsync	Vertical Synchronisation Signal
DE	Display Enable Signal
Pixelclock	Reference Clock for Individual Pixels
Bitclock	Internal Clock used to derive subclocks like Pixelclock
PixelFiFo	Buffer for incoming Pixellink data working with FiFo method
Hdelay	Programmable delay value for the PixelFiFo
Pixellink	Part of APIX [®] technology transmitting video data
APIX [®]	Automotive Pixel Link by Inova Semiconductors
TX	Transmitter
RX	Receiver
Ndiv	Divider value N for nominal frequency N = 2 ... 255
Pdiv	Divider value P for nominal frequency P = 0 ... 4
Psub	sub P value to set frequencies between N and P
HU	HeadUnit – also used as term for the transmitting side of the video data stream