

FUJITSU SEMICONDUCTOR

MB88F332

**FLASH Memory Product
Parallel Writer Specification**

Ver.1.0

FUJITSU MICROELECTRONICS LIMITED

【Revision History】

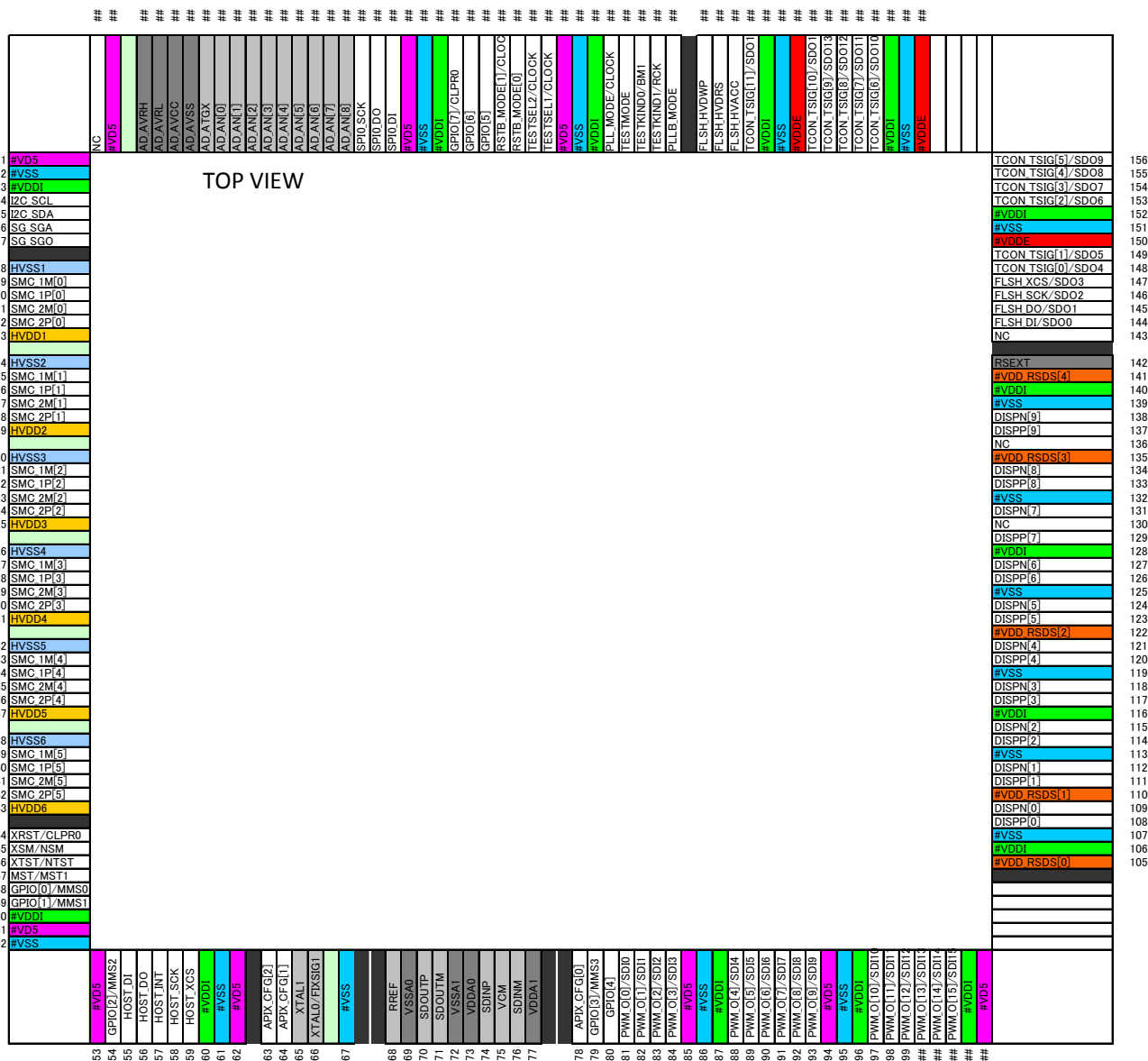
Ver.	Data	Description
1.0	2008/12/16	First Editinon

【Overview】

Items	Detail	Reference
Product name	MB88F332	
FLASH memory size	160KB	
Sector configuration		添付 01:1 項
Start/End address	Start address :58000 _H End address :7FFFF _H	
Compatible product info	—	
Package info.	FPT-208P-M06 (LQFP)	添付 02
IC socket info.	Open-top-type: IC201-001 (Yamaitchi)	
Pin Assignment Diagram	—	添付 01:2 項
Pin Functions	—	添付 01:3,4 項
DC characteristics	—	添付 01:5 項
FLASH Memory Write/Erase characteristics	—	添付 01:6 項
AC characteristics	—	添付 01:7 項
FLASH Memory specification	—	添付 03
Sector protect fnctioin	—	
Security function	—	

2 Pin Assignment Diagram

■LQFP-208



3 Pin Functions

Pin number LQFP	Pin name (*1)	Built-in Pull up/down	Parallel writer mode Pin function			
			Pin name	Function	Connection	Input/Output level
102	PWM_O[15]	—	DQ15	Data input/output	Parallel writer	CMOS
101	PWM_O[14]	—	DQ14	Data input/output	Parallel writer	
100	PWM_O[13]	—	DQ13	Data input/output	Parallel writer	
99	PWM_O[12]	—	DQ12	Data input/output	Parallel writer	
98	PWM_O[11]	—	DQ11	Data input/output	Parallel writer	
97	PWM_O[10]	—	DQ10	Data input/output	Parallel writer	
93	PWM_O[9]	—	DQ9	Data input/output	Parallel writer	
92	PWM_O[8]	—	DQ8	Data input/output	Parallel writer	
91	PWM_O[7]	—	DQ7	Data input/output	Parallel writer	
90	PWM_O[6]	—	DQ6	Data input/output	Parallel writer	
89	PWM_O[5]	—	DQ5	Data input/output	Parallel writer	
88	PWM_O[4]	—	DQ4	Data input/output	Parallel writer	
84	PWM_O[3]	—	DQ3	Data input/output	Parallel writer	
83	PWM_O[2]	—	DQ2	Data input/output	Parallel writer	
82	PWM_O[1]	—	DQ1	Data input/output	Parallel writer	
81	PWM_O[0]	—	DQ0	Data input/output	Parallel writer	
186	GPIO[7]	—	BYTEX	Byte access enable input	Parallel writer	CMOS hysteresis level
185	GPIO[6]	—	RSTX	Reset input	Parallel writer	
184	GPIO[5]	—	CEX	Chip enable input	Parallel writer	
80	GPIO[4]	—	WEX	Write enable input	Parallel writer	
79	GPIO[3]	—	OEX	Output enable input	Parallel writer	
54	GPIO[2]	—	TESTX	Mode input	pull-up	
49	GPIO[1]	—	ATDIN	Test signal input	Parallel writer	
48	GPIO[0]	—	EQIN	Test signal input	Parallel writer	
191	SPI0_DO	—	AQ18	Address input	Parallel writer	
190	SPI0_DI	—	AQ17	Address input	Parallel writer	
192	SPI0_SCK	—	AQ16	Address input	Parallel writer	
183	RSTB_MODE[1]	—	AQ15	Address input	Parallel writer	
182	RSTB_MODE[0]	—	AQ14	Address input	Parallel writer	
181	TESTSEL2	—	AQ13	Address input	Parallel writer	
180	TESTSEL1	—	AQ12	Address input	Parallel writer	

176	PLL_MODE	—	AQ11	Address input	Parallel writer	
168	TCON_TSIG[11]	—	AQ10	Address input	Parallel writer	
164	TCON_TSIG[10]	—	AQ9	Address input	Parallel writer	
163	TCON_TSIG[9]	—	AQ8	Address input	Parallel writer	
162	TCON_TSIG[8]	—	AQ7	Address input	Parallel writer	
161	TCON_TSIG[7]	—	AQ6	Address input	Parallel writer	
160	TCON_TSIG[6]	—	AQ5	Address input	Parallel writer	
156	TCON_TSIG[5]	—	AQ4	Address input	Parallel writer	
155	TCON_TSIG[4]	—	AQ3	Address input	Parallel writer	
154	TCON_TSIG[3]	—	AQ2	Address input	Parallel writer	
153	TCON_TSIG[2]	—	AQ1	Address input	Parallel writer	
149	TCON_TSIG[1]	—	AQ0	Address input	Parallel writer	
148	TCON_TSIG[0]	—	RDY	Ready output	Parallel writer	CMOS (擬似 Nch オープンドレイン)
169	FLSH_HVACC	—	HVACC	Mode input	pull-up	CMOS hysteresis level
170	FLSH_HVDRS	—	HVDRS	Mode input	pull-up	
171	FLSH_HVDWP	—	HVDWP	Mode input	pull-up	
65	XTAL0	—	X0	Oscillation pin	pull-down	
66	XTAL1	—	X1	Oscillation pin	OPEN	
78	APIX_CFG[0]	—	CLK	Clock Input	10MHz Clock	
1, 13, 19, 25, 31, 37, 43, 51, 53, 62, 85, 94, 104, 179, 189, 207	VCC3	—		Power(5.0V)	Power(5.0V)	—
105, 110, 122, 135, 141, 150, 157, 165	VCC2	—		Power(3.3V)	Power(3.3V)	—
3, 50, 60, 73, 77, 87, 96, 103, 106, 116, 128, 140, 152, 159, 167, 177, 187	VCC1	—		Power (1.8V)	Power(1.8V)	—
2, 8, 14, 20, 26, 32, 38, 52, 61, 67, 69, 72, 86, 95, 107, 113, 119, 125, 132, 139, 151, 158, 166, 178, 188	VSS	—		GND	GND	—
206	AD_AVRH	—		Analog reference voltage input	Power(5.0V)	—
205	AD_AVRL	—		Analog reference voltage input	GND	—
204	AD_AVCC	—		Analog Power	Power(5.0V)	—
203	AD_AVSS	—		Analog GND	GND	—
other	other	—		Unused	OPEN	—

*1: 通常端子名に付いては、表記のスペース上、リソースおよびアナログ入出力記号は省略しています。

4 DC characteristics

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Power supply current	ICC	VCC	VCC=1.9V fc=25MHz 書込み時	—	37.5	-	mA
			VCC=1.9V fc=25MHz 読出し時	—	15	40	mA
			VCC=1.9V fc=25MHz 消去時	—	15	40	mA
“H” level input voltage	VIH	Other input pin and inoutput pin (*1)	—	$0.8 \times VCC3$	—	$VCC3 + 0.5$	V
		TCON_TSIG[11:0]	—	$0.8 \times VCC2$	—	$VCC2 + 0.3$	V
“L” level input voltage	VIL	Other input pin and inoutput pin (*1)	—	VSS	—	$0.2 \times VCC3$	V
		TCON_TSIG[11:0]	—	VSS	—	$0.2 \times VCC2$	V
“H” level output voltage	VOH	All output pin	—	$VCC3 - 0.4$	—	—	V
“L” level output voltage	VOL	All output pin	—	—	—	0.4	V

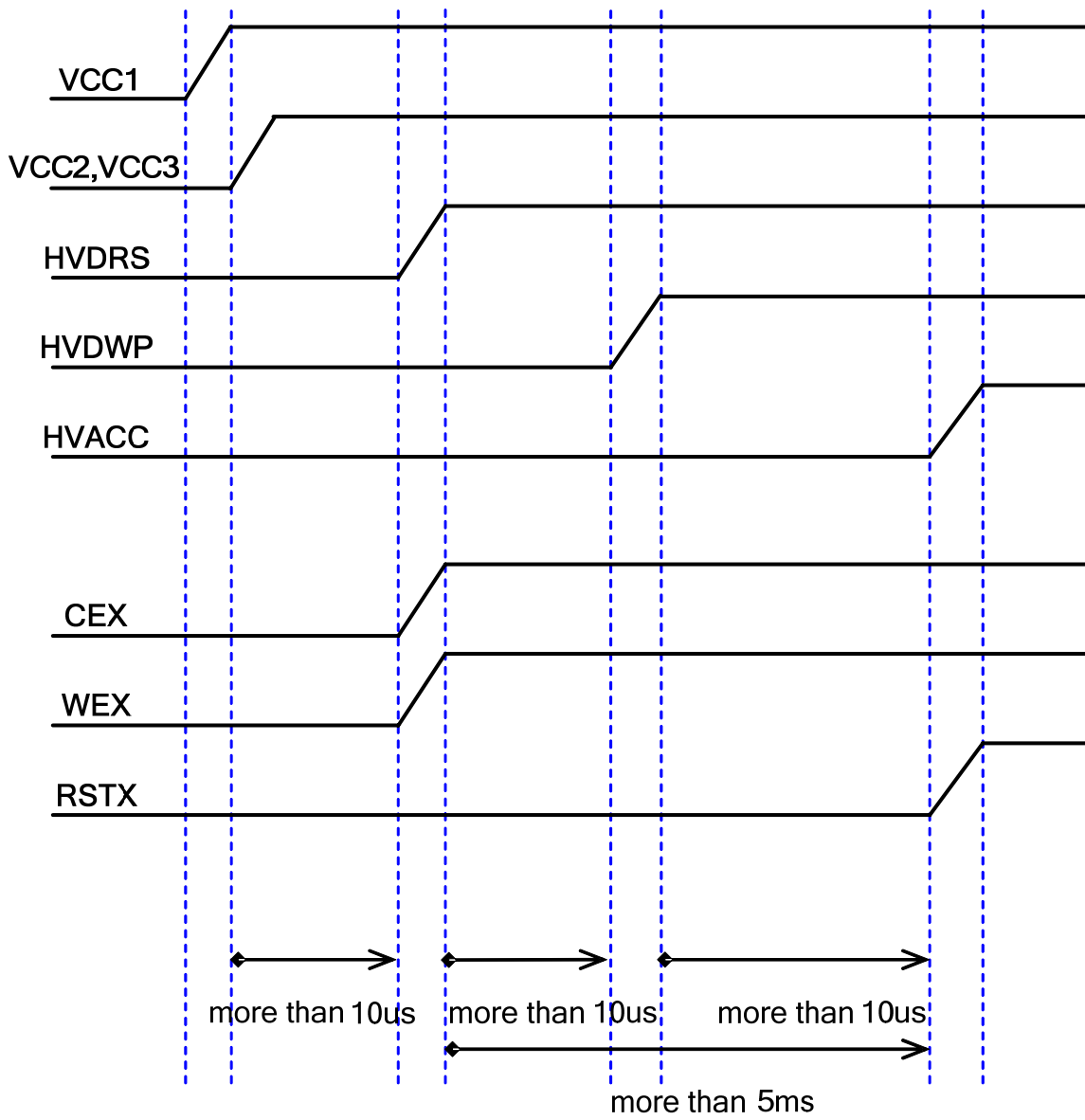
*1: PWM_O[15:0],GPIO[7:0],SPI0_DO,SPI0_DI,SPI0_SCK,RSTB_MODE[1:0],TESTSEL2,TESTSEL1,PLL_MODE

5 FLASH Memory Write/Erase characteristics

■ MB88F332

Parameter	conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Ta=+25°C V _{CC} =3.3V	—	0.9	3.6	s	Excluding the internal pre-program time
word(16bit) write time		—	23	370	μs	Excluding the system overhead time
Erase/write cycles	—	100000	—	—	cycle	at T _j <105C / 10,000cycle at T _j >105C

6 AC characteristics



Revision History

	Date	Description
1.0	2008.12.16	o First revision

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1. DEVICE BUS OPERATIONS

1.1. Byte Mode (BYTEX=L)

User Bus Operations Table (BYTEX = VIL)

Operation	CEX	OEX	WEX	DQ7 to DQ0	RSTX	HVDWP	HVDRS	HVACC
Read ^{*1}	L	L	H	DOUT	H	H	H	H
Standby	H	X	X	High-Z	H	H	H	H
Output Disable	L	H	H	High-Z	H	H	H	H
Write (Program/Erase)	L	H	L	DIN	H	H	H	H
Reset (Hardware) / Standby	X	X	X	High-Z	L	H	H	H

Legend: L = VIL, H = VIH, X = VIL or VIH, Legend: L = VIL, H = VIH, X = VIL or VIH,

*1: WEX can be VIL if OEX is VIL, OEX at VIH initiates the write operations.

1.2. Word Mode (BYTEX=H)

User Bus Operations Table (BYTEX = VIH)

Operation	CEX	OEX	WEX	DQ15 to DQ0	RSTX	HVDWP	HVDRS	HVACC
Read ^{*1}	L	L	H	DOUT	H	H	H	H
Standby	H	X	X	High-Z	H	H	H	H
Output Disable	L	H	H	High-Z	H	H	H	H
Write (Program/Erase)	L	H	L	DIN	H	H	H	H
Reset (Hardware) / Standby	X	X	X	High-Z	L	H	H	H

Legend: L = VIL, H = VIH, X = VIL or VIH, Legend: L = VIL, H = VIH, X = VIL or VIH,

*1: WEX can be VIL if OEX is VIL, OEX at VIH initiates the write operations.

2. COMMAND DEFINITIONS

2.1. Standard Command Definitions

Standard Command Definitions

Command Sequence	Bus Write Cycles	1st. Bus Write Cycle		2nd. Bus Write Cycle		3rd. Bus Write Cycle		4th. Bus Read/Write Cycle		5th. Bus write Cycle		6th. Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset ^{*1}	1	X	F0	RA	RD								
Read/Reset ^{*1}	3	AA8	AA	554	55	AA8	F0	RA	RD				
Program	4	AA8	AA	554	55	AA8	A0	PA	PD				
Chip Erase	6	AA8	AA	554	55	AA8	80	AA8	AA	554	55	AA8	10
Sector Erase	6	AA8	AA	554	55	AA8	80	AA8	AA	554	55	SA	30
Sector Erase Suspend	1	X	B0										
Sector Erase Resume	1	X	30										

RA: Address of the memory location to be read, RD: Data read from location RA during read operation.

PA: Address of the memory location to be programmed, PD: Data to be programmed at location PA..

SA: Address of the sector to be erased. (Any address in the sector to be erased)

X: don't care

All values are in Hex.

Valid address of the commands are from AQ11 to AQ2. Others are not cared.

*1: Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

2.2. Extended Command Definitions

Extended Command Definitions

Extended Command Sequence	Bus Write Cycles	1st. Bus Write Cycle		2nd. Bus Write Cycle		3rd. Bus Write Cycle		4th. Bus Read Cycle	
		Address	Data	Address	Data	Address	Data	Address	Data
Set to Fast Mode	3	AA8	AA	554	55	AA8	20		
Fast Program ^{*1}	2	X	A0	PA	PD				
Reset from Fast Mode ^{*1}	2	X	90	X	F0 ^{*2}				

PA: Address of the memory location to be programmed, PD: Data to be programmed at location PA..

X: don't care

All values are in Hex.

Valid address of the commands are from AQ11 to AQ2. Others are not cared.

*1: This command is valid while Fast Mode.

*2: This data "00h" is also acceptable.

3. FUNCTIONAL DESCRIPTION

3.1. Bus Operations

(1) Read

The Embedded Flash have two control functions which must be satisfied in order to obtain data at the outputs. CEX is the power control and should be used for a device selection. OEX is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable CEX to valid data at the output pins. The output enable access time is the delay from the falling edge of OEX to valid data at the output pins. (Assuming the addresses have been stable for at least $t_{ACC-t_{OE}}$ time.) When reading out a data without changing addresses after power-up, it is necessary to input hardware reset or change CEX pin from VIH or VIL

In addition, there is a limitation of address change order. When reading out a data with address changing, it is necessary that change occur on one of AQ0, AQ1, AQ2, AQ3. Changing on the other address pins should occur within t_{AA} before AQ0, AQ1, AQ2 or AQ3 changed.

(2) Standby

There are two ways to implement the standby mode on the Embedded Flash devices, one using both the CEX and RSTX pins; the other via the RSTX pin only.

When using both pins, a CMOS standby mode is achieved with CEX and RSTX inputs both held at VIH. Under this condition the current consumed is less than 5 μ A. The device can be read with standard access time (t_{CE}) from either of these standby modes. During Embedded Algorithm operation, VCC active current is required even CEX = VIH.

When using the RSTX pin only, a CMOS standby mode is achieved with RSTX input held at VIL (CEX = VIH or VIL). Under this condition the current is consumed is less than 5 μ A. Once the RSTX pin is taken high, the device requires t_{RH} of wake up time before outputs are valid for read access.

In the standby mode the outputs are in the high impedance state, independent of the OEX input.

(3) Automatic Sleep

There is a function called automatic sleep mode to restrain power consumption during read-out of Embedded Flash data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To activate this mode, Embedded Flash automatically switch themselves to low power mode when Embedded Flash addresses remain stable for $t_{ACC} + 30$ ns. It is not necessary to control CEX, WEX, and OEX on the mode. Under the mode, the current consumed is typically 1 μ A (CMOS Level).

Since the data are latched during this mode, the data are read-out continuously. If the addresses are changed, the mode is canceled automatically and Embedded Flash read-out the data for changed addresses.

(4) Output Disable

With the OEX input at a logic high level (VIH), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

(5) Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the

commands, along with the address and data information needed to execute the command. The command register is written by bringing WEX to VIL, while CEX is at VIL and OEX is at VIH. Addresses are latched on the falling edge of WEX or CEX, whichever happens later; while data is latched on the rising edge of WEX or CEX, whichever happens first. Standard microprocessor write timings are used. Refer to 5.2.~5.4 Write Access.

(6) Reset

The Embedded Flash devices may be reset by driving the RSTX pin to VIL. The RSTX pin has a pulse requirement and has to be kept low (VIL) for at least 500 ns in order to properly reset the internal state machine.

Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode 20 us after the RSTX pin is driven low. Furthermore, once the RSTX pin goes high, the devices require an additional t_{RH} before it will allow read access. When the RSTX pin is low, the devices will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/BYX output signal should be ignored during the RSTX pulse. See 5.8. RY/BYX Signal Output.

If hardware reset occurs during Embedded Erase Algorithm, there is a possibility that the erasing sector(s) cannot be used.

3.2. Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the devices to the read mode. 2.1. Standard Command Definitions Table defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Moreover both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ0 to DQ7 and DQ8 to DQ15 bits are ignored.

(1) Read/Reset Command

In order to return from Read Sector Protect mode or Exceeded Timing Limits (DQ5 = 1) to read/reset mode, the read/reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The devices remain enabled for reads until the command register contents are altered.

The devices will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the 5. TIMING DIAGRAM for the specific timing parameters.

(2) Byte/Word Programming

The devices are programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of CEX or WEX, whichever happens later and the data is latched on the rising edge of CEX or WEX, whichever happens first. The rising edge of CEX or WEX (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit at which time the devices return to the read mode and addresses are no longer latched. (See “Hardware Sequence Flags Table” in 3.3.(1).) Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance of time. Hence, Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored. If hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from read/reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

(3) Chip Erase

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the devices will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase (Preprogram function). The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last WEX pulse in the command sequence and terminates when the data on DQ7 is “1” (See “3.3.(2) DQ7”). at which time the device returns to read the mode.

Chip Erase Time; Sector Erase Time * All sectors + Chip Program Time (Preprogramming)

(4) Sector Erase

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Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of WEX, while the command (Data=30h) is latched on the rising edge of WEX. After time-out of 80 us from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on 2.1. Standard Command Definitions. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80 us otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 us from the rising edge of the last WEX will initiate the execution of the Sector Erase command(s). If another falling edge of the WEX occurs within the 80 us time-out window the timer is reset. (Monitor DQ3 to determine if the sector erase timer window is still open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the devices to the read mode, ignoring the previous command string. Resetting the devices once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to “3.3. Write Operation Status” for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors.

Sector erase does not require the user to program the devices prior to erase. The devices automatically program all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the 80 us time out from the rising edge of the WEX pulse for the last sector erase command pulse and terminates when the data on DQ7 is “1” (See “3.3. Write Operation Status”.) at which time the devices return to the read mode. Data polling must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] * Number of Sector Erase

(5) Erase Suspend

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writing the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command resumes the erase operation. The addresses are DON'T CARES when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 20 us to suspend the erase operation. When the devices have entered the erase-suspended mode, the RY/BYX output pin and the DQ7 bit will be at logic “1”, and DQ6 will stop toggling. The user must use the address of the erasing sector for reading DQ6 and DQ7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the devices default to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ2 to toggle. (See the section on DQ2.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the devices are in the erase-suspend-program mode will cause DQ2

to toggle. The end of the erase-suspended Program operation is detected by the RY/BYX output pin, Data polling of DQ7, or by the Toggle Bit I (DQ6) which is the same as the regular Program operation. Note that DQ7 must be read from the Program address while DQ6 can be read from any address.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

3.3. Write Operation Status

(1)Hardware Sequence Flags

Status		DQ7	DQ6	DQ5	DQ3	DQ2	
In Progress	Embedded Program Algorithm	~DQ7	Toggle	0	0	1	
	Embedded Erase Algorithm (Erase Suspended Sector)	0	Toggle	0	1	Toggle	
	Embedded Erase Algorithm (Non-Erase Suspended Sector)	0	Toggle	0	1	1	
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
	Erase Suspend Program (Non-Erase Suspended Sector)	~DQ7	Toggle	0	0	1	
Exceeded Time Limits	Embedded Program Algorithm	~DQ7	Toggle	1	0	1	
	Embedded Erase Algorithm	0	Toggle	1	1	N/A	
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	~DQ7	Toggle	1	0	N/A

(2)DQ7

~Data Polling

The Embedded Flash devices feature Data Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the devices will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a “1” at the DQ7 output.

For chip erase and sector erase, the Data Polling is valid after the rising edge of the sixth WEX pulse in the six write pulse sequence. Data Polling must be performed at sector address within any of the sectors being erased. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the Embedded Flash data pins (DQ7) may change asynchronously while the output enable (OEX) is asserted low. This means that the devices are driving status information on DQ7 at one instant of time and then that byte’s valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ7 has a valid data, the data outputs on DQ0 to DQ6 may be still invalid. The valid data on DQ0 to DQ7 will be read on the successive read attempts.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. See 3.3.(1)Hardware Sequence Flags

(3)DQ6

Toggle Bit I

The Embedded Flash also feature the “Toggle Bit I” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read (OEX toggling) data from the devices will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth WEX pulse in the four write pulse sequence.

For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth WEX pulse in the six write pulse sequence. The Toggle Bit I is active during the sector time out.

Either CEX or OEX toggling will cause the DQ6 to toggle. In addition, an Erase Suspend/Resume command will cause the DQ6 to toggle.

(4)DQ5

Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data Polling is the only operating function of the devices under this condition. The CEX circuit will partially power down the device under these conditions (to approximately 2 mA).

The OEX and WEX pins will control the output disable functions as described in User Bus Operations Tables in 1. DEVICE BUS OPERATIONS.

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the devices lock out and never complete the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the devices have exceeded timing limits, the DQ5 bit will indicate a “1.” Please note that this is not a device failure condition since the devices were incorrectly used. If this occurs, reset the device with command sequence.

(5)DQ3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high (“1”) the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit I. If DQ3 is low (“0”), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent Sector Erase command. If DQ3 were high on the second status check, the command may not have been accepted. See 3.3.(1) Hardware Sequence Flags.

(6)DQ2

This toggle bit II, along with DQ6, can be used to determine whether the devices are in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ2 to toggle during the Embedded Erase Algorithm. If the devices are in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ2 to toggle. When the devices are in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic “1” at the DQ2 bit.

DQ6 is different from DQ2 in that DQ6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ7, is summarized as follows: For example, DQ2 and DQ6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ2 toggles while DQ6 does not.) See 3.3.(1) Hardware Sequence Flags.

Furthermore, DQ2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ2 toggles if this bit is read from an erasing sector.

(7)RDY

Ready/~Busy

The Embedded Flash provide a RDY open-drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the devices are busy with either a program or erase operation. If the output is high, the devices are ready to accept any read/write or erase operation. When the RDY pin is low, the devices will not accept any additional program or erase commands. If the Embedded Flash are placed in an Erase Suspend mode, the RDY output will be high.

During programming, the RDY pin is driven low after the rising edge of the fourth WEX pulse. During an erase operation, the RDY pin is driven low after the rising edge of the sixth WEX pulse. The RDY pin will indicate a busy condition during the RSTX pulse. Refer to 5.7. RDY signal output.

The RDY pin is pulled high in standby mode.

Since this is an open-drain output, RDY pins can be tied together in parallel with a pull-up resistor to VCC.

3.4. Data Protection

The Embedded Flash are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the devices automatically reset the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The devices also incorporate several features to prevent inadvertent write cycles resulting form VCC power-up and power-down transitions or system noise.

3.5. Low VCC Write Inhibit

To avoid initiation of a write cycle during VCC power-up and power-down, a write cycle is locked out for VCC less than 1.2 V (typically 1.4 V). If $VCC < VLKO$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the VCC level is greater than VLKO. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when VCC is above 1.2 V.

If Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector(s) cannot be used.

3.6. Write Pulse “Glitch” Protection

Noise pulses of less than 3 ns (typical) on OEX, CEX, or WEX will not initiate a write cycle.

3.7. Logical Inhibit

Writing is inhibited by holding any one of $OEX = VIL$, $CEX = VIH$, or $WEX = VIH$. To initiate a write cycle CEX and WEX must be a logical zero while OEX is a logical one.

3.8. Power-Up Write Inhibit

Power-up of the devices with $WEX = CEX = VIL$ and $OEX = VIH$ will not accept commands on the rising edge of WEX.

The internal state machine is automatically reset to the read mode on power-up.

3.9. Extended Command

(1) Fast Mode

Embedded Flash has Fast Mode function. This mode dispenses with the initial two unlock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. The VCC active current is required even $CEX = VIH$ during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD).

4. AC CHARACTERISTICS

4.1. Read access

(In a recommended operating condition)

Item	Symbol	Condition	Value			Unit
			MIN	TYP	MAX	
Read Cycle Time	t_{RC}	---	35.0	---	---	ns
Address Access Time	t_{ACC}	CEX=VIL OEX=VIL	---	---	120	ns
CEX to Data output	t_{CE}	---	---	---	120	ns
OEX to Data output	t_{OE}	---	---	---	10	ns
CEX to Output Hi-z	t_{DF}	---	---	---	10	ns
OEX to Output Hi-z	t_{DF}	---	---	---	10	ns
Output Hold Time of pre-cycle Data	t_{OH}	---	0	---	---	ns
RSTX Pin Low to Read Mode	t_{Ready}	---	---	---	20	us
Other address change to AQ0, AQ1, AQ2, AQ3 change	t_{AA}	CEX=VIL	0	---	---	ns

4.2. Write access

(In a recommended operating condition)

Item		Symbol	Value			Unit
			MIN	TYP	MAX	
Write Access Time		t_{WC}	80	---	---	ns
Address Setup Time		t_{AS}	0	---	---	ns
Address Hold Time		t_{AH}	45	---	---	ns
Data Setup Time		t_{DS}	45	---	---	ns
Data Hold Time		t_{DH}	0	---	---	ns
Output Enable Setup Time		t_{OES}	0	---	---	ns
Output Enable Hold Time	Read	t_{OEHL}	0	---	---	ns
	Toggle and Data Polling		10	---	---	ns
Read Recover Time Before Write		t_{GHWL}	0	---	---	ns
CEX Setup Time		t_{CS}	0	---	---	ns
CEX Hold Time		t_{CH}	0	---	---	ns
Write Pulse Width		t_{WP}	50	---	---	ns
Write Pulse Width High		t_{WPH}	30	---	---	ns
Read Recover Time Before Write		t_{GHHL}	0	---	---	ns
WEX Setup Time		t_{WS}	0	---	---	ns
WEX Hold Time		t_{WH}	0	---	---	ns
CEX Pulse Width		t_{CP}	50	---	---	ns
CEX Pulse Width High		t_{CPH}	30	---	---	ns
Byte Programming Operation		t_{WHWH1}	---	15 *2	---	us
Sector Erase Operation *1		t_{WHWH2}	---	0.9 *3	---	sec
RSTX Pulse Width		t_{RP}	500	---	---	ns
RSTX Hold time before read		t_{RH}	200	---	---	ns
Program/Erase Valid to RY/BYX Delay		t_{BUSY}	90	---	---	ns

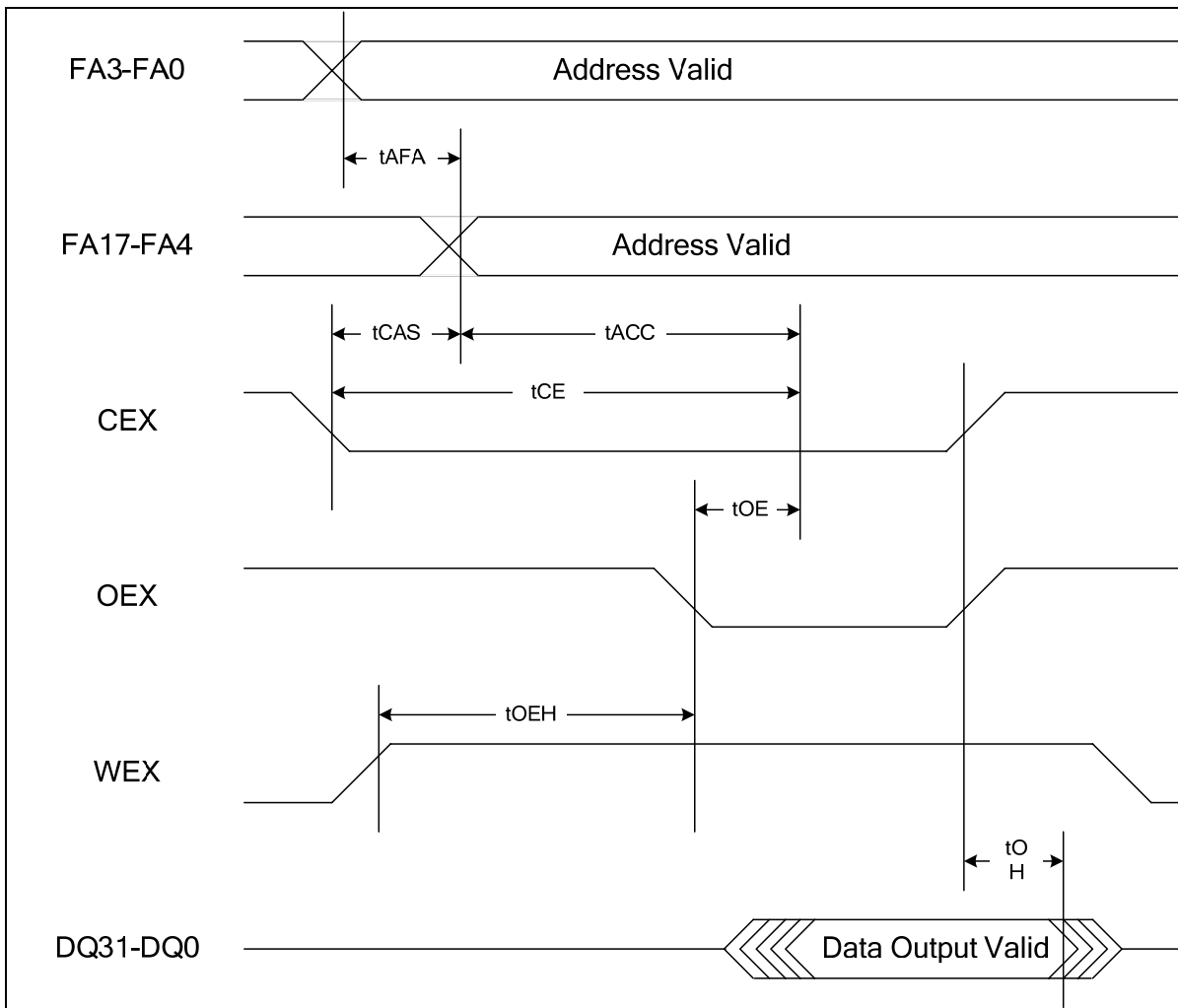
*1 : This does not include the preprogramming time.

*2 : Low End Macro : 15 us

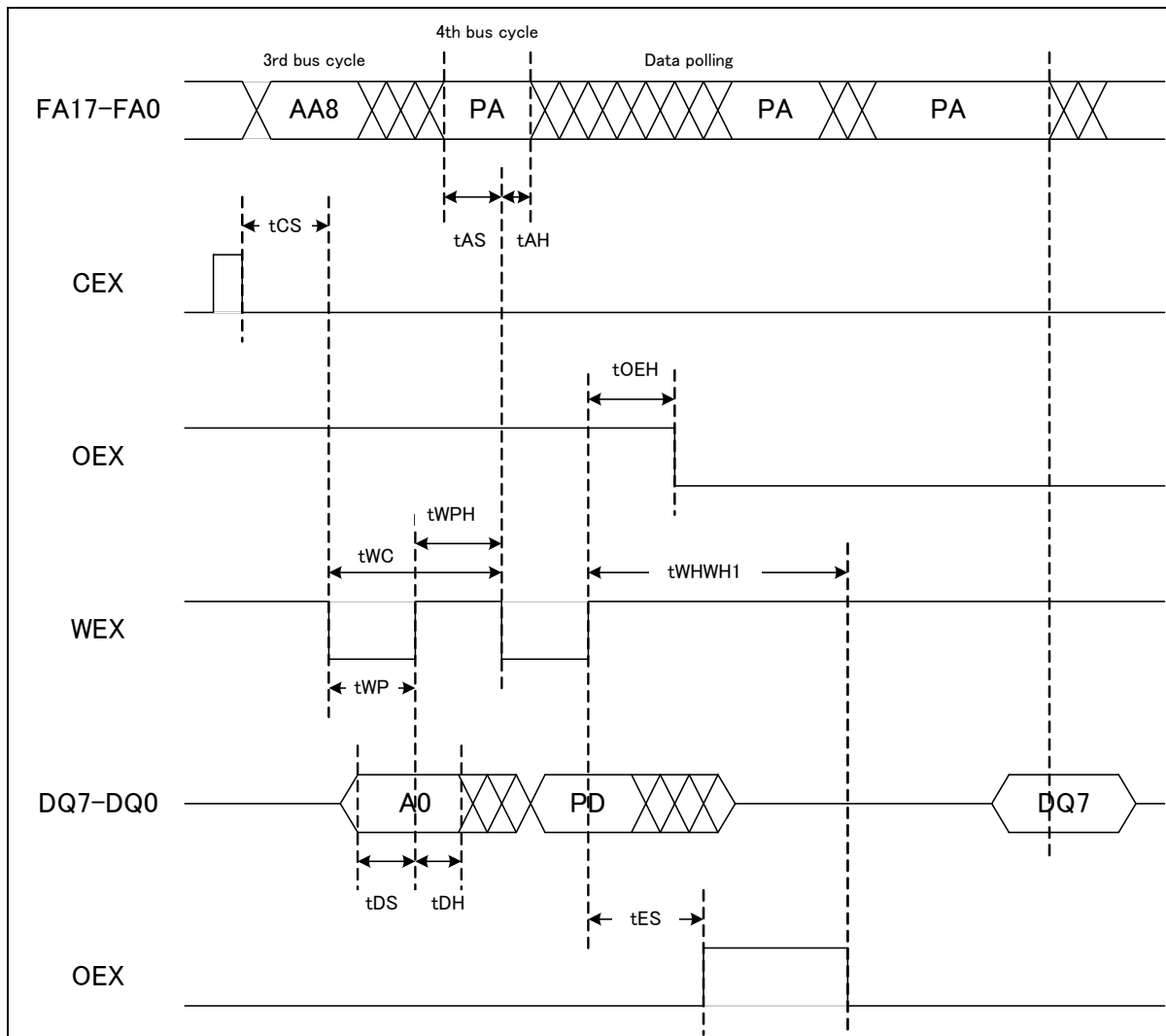
*3 : Low End Macro : 0.9 sec

5. TIMING DIAGRAM

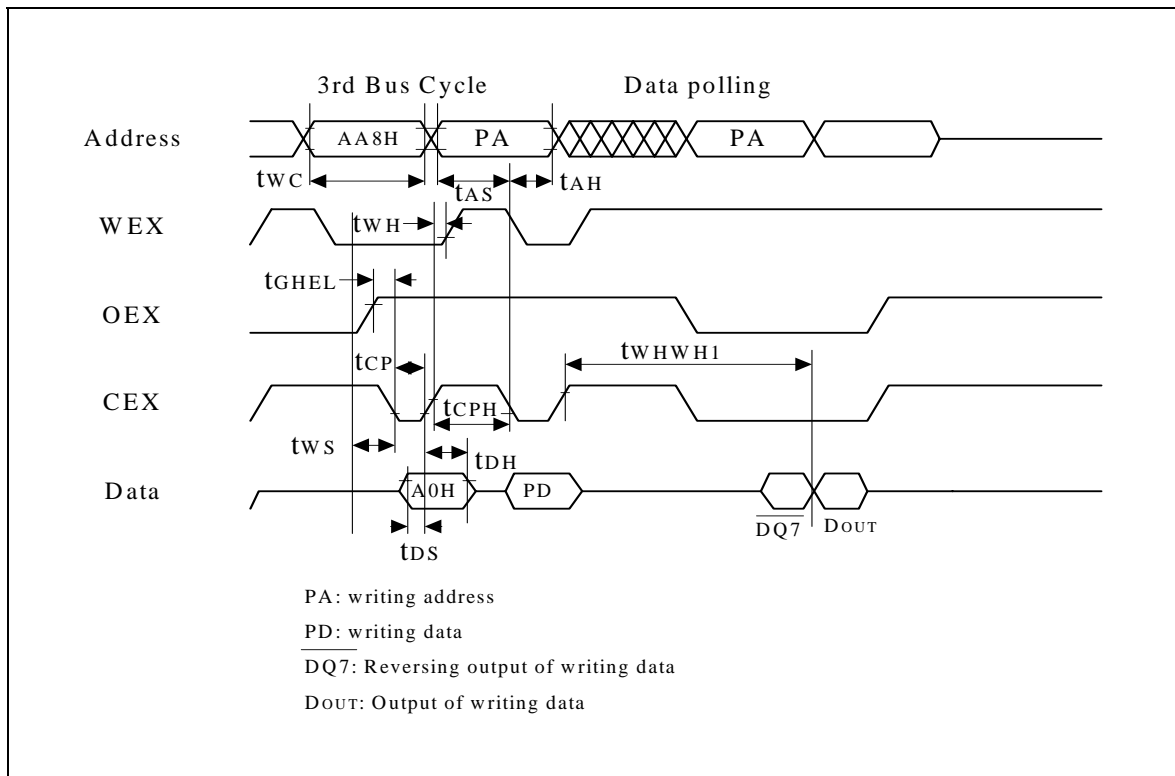
5.1. Reading of data by read access



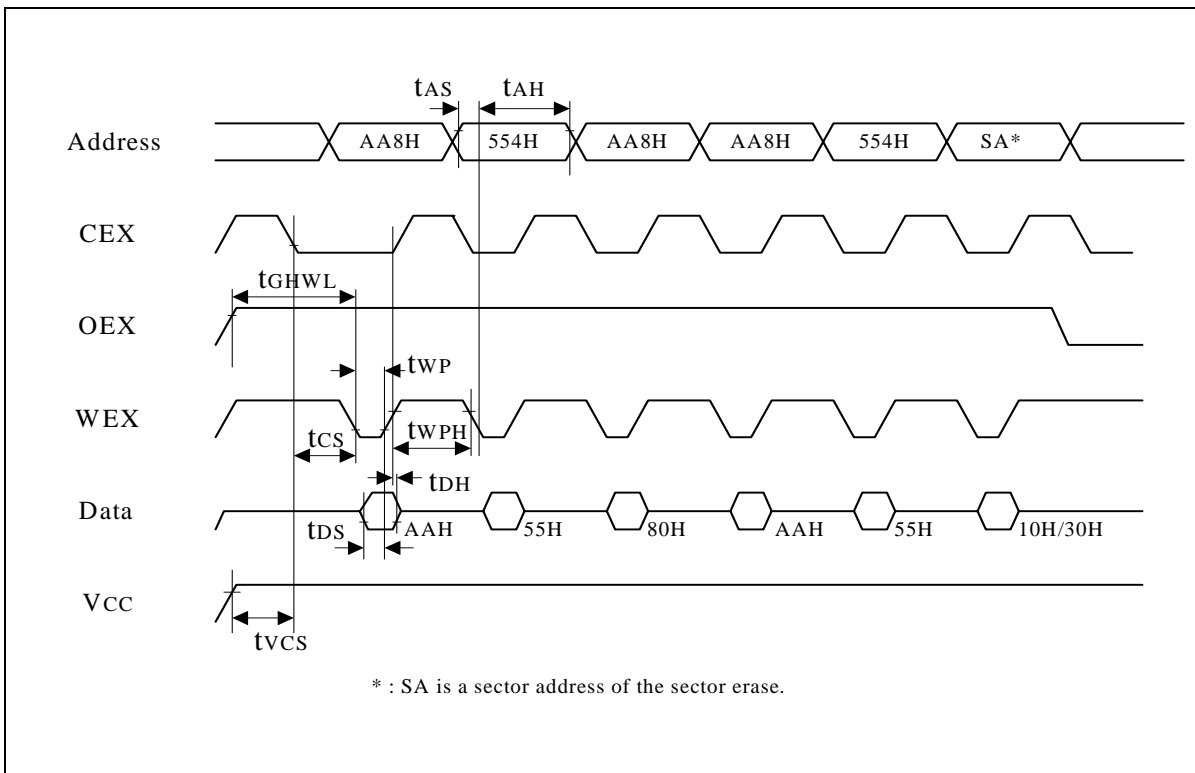
5.2. Write access – Data polling – Read access (WEX control)



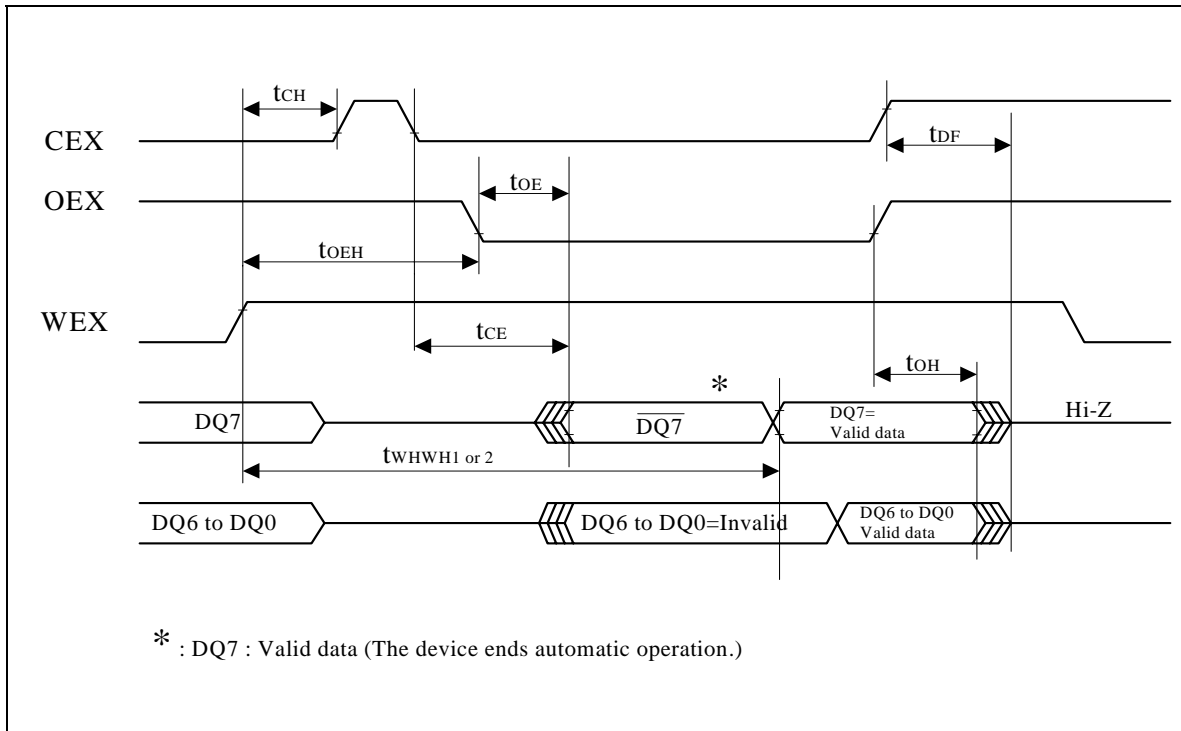
5.3. Write access – Data polling – Read access (CEX control)



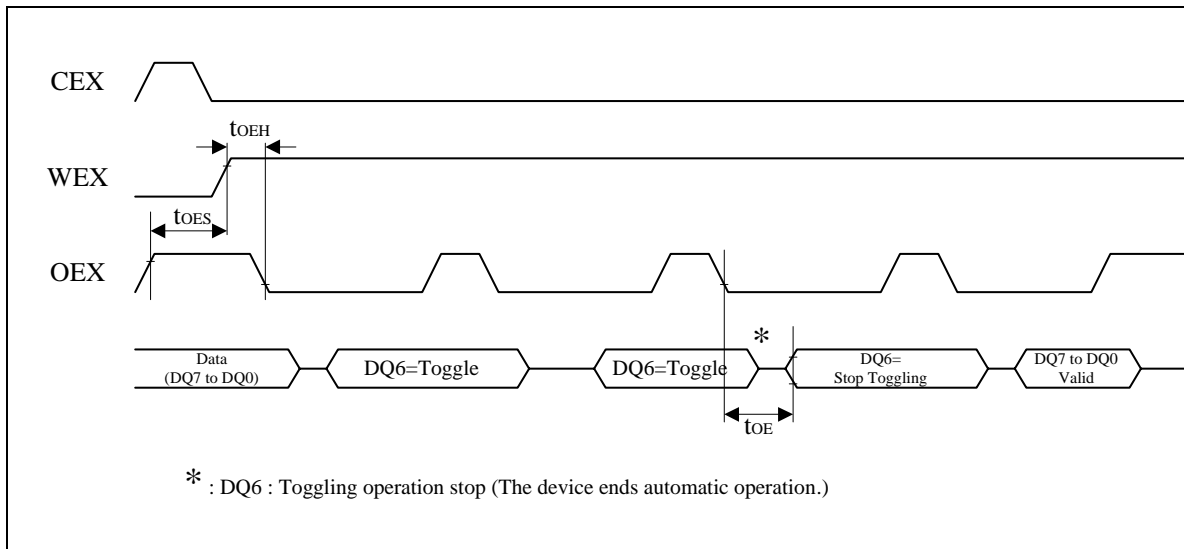
5.4. Write access (Erase the chip / Sector erase)



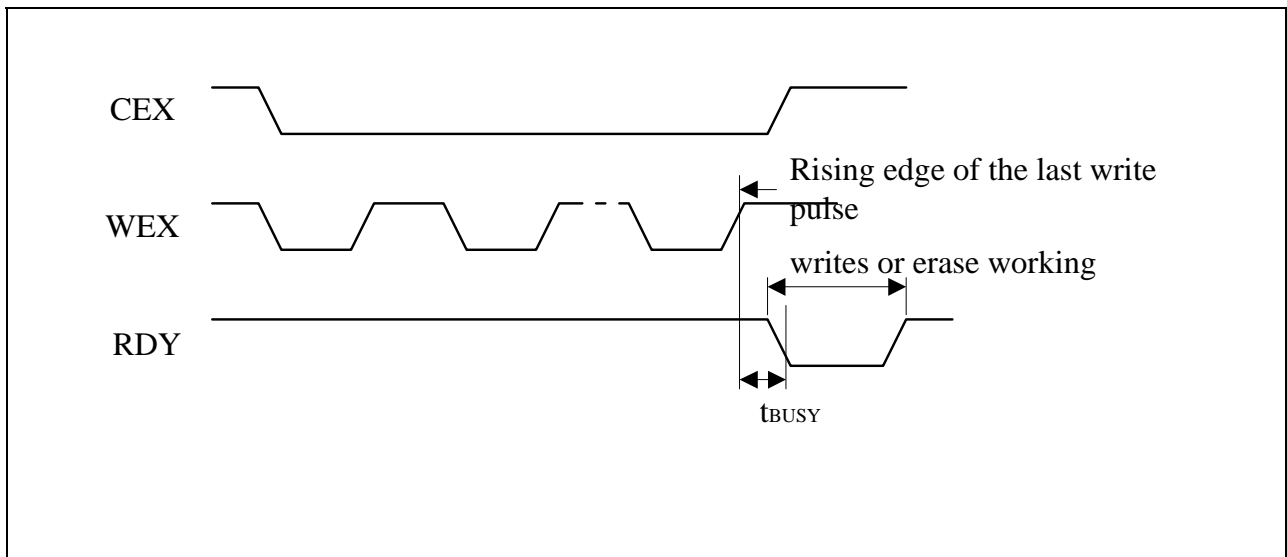
5.5. Data polling



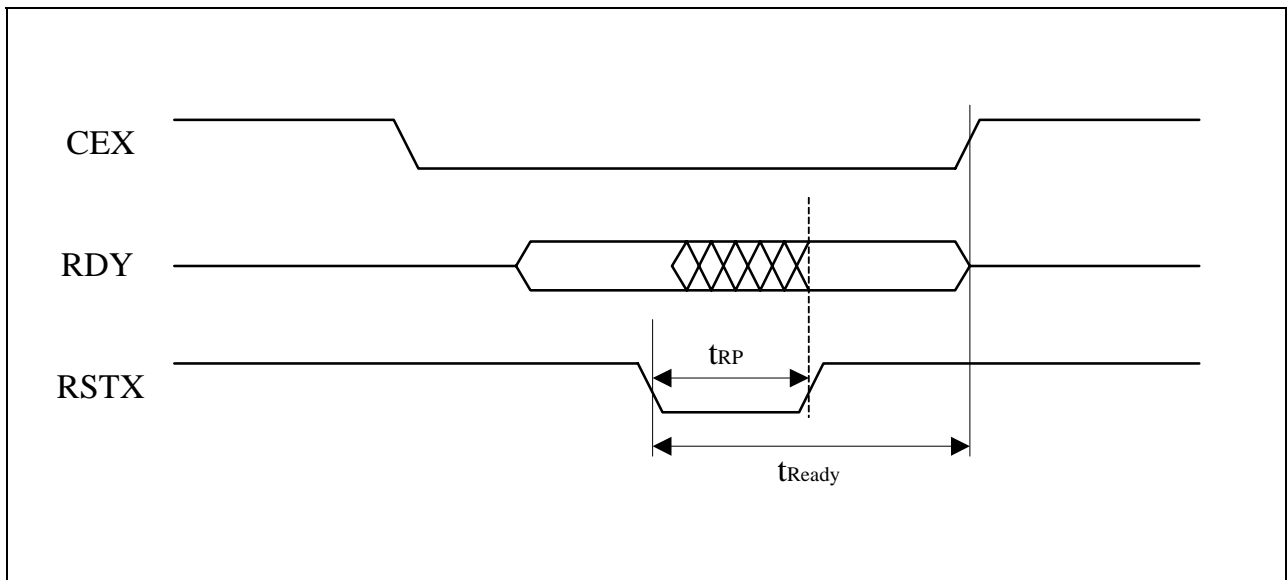
5.6. Toggle bit



5.7. RDY signal output (Write/Erase operation)



5.8. RDY signal output (Hardware Reset)



5.9. Limited Address Change Order

