

MB88F332 'Indigo' APIX Layout Recommendations

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History

Date	Author	Version	Comment
17.03.2009	GCC/HA	0.01	First draft version
01.04.2009	HA	0.02	First release
21.08.2009	AvT	0.03	Modification to figure 3-3 (ferrite instead of 0R between APIX GND and GND)

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1 Abstract

This document provides recommendations for the layout of the APIX interface and its differential signals. In addition, some critical components are described and requirements for the power supply module are discussed. Reference Designs (schematic and layout) can be purchased directly from Inova Semiconductors for extensive testing, measuring and evaluation. This application note supports designers and answers the most common questions. It is not intended to replace the designer's own responsibility nor can it guarantee optimized operation conditions.

2 General Description

The MB88F332 'Indigo' GDC uses the **Automotive Pixel Link (APIX)** from Inova Semiconductors as an interface to other Fujitsu controllers as well as to discrete transmitters from Inova Semiconductors or other graphic controller/processor products with an integrated APIX interface. Due to the fact that the APIX interface currently uses a serial link with up to 1 GB/s transfer rate, it is mandatory to obey certain rules for the layout and when selecting components.

3 The Layout

General layout rules for differential high speed signals should be taken into consideration. In addition, it is recommended to design the layout with these main parameters:

- Transmission line differential impedance is: $Z_0 = 100 \text{ Ohm}$.
- Transmission line single-ended impedance is 50 Ohms to APIX GND.
- Make sure that a differential pair has equal line lengths.
- Route APIX GND under traces.
- Maintain equal gaps on the whole trace.
- Avoid sharp corners in traces.
- Avoid cross-talk – keep pairs away from other signals or shield APIX GND.

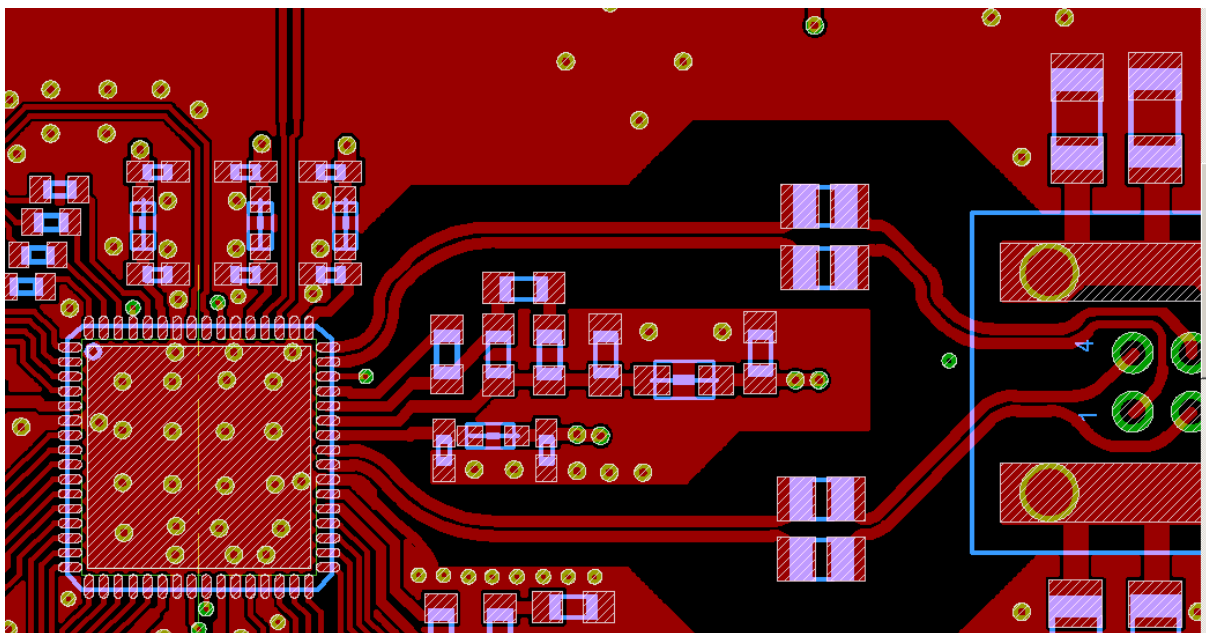
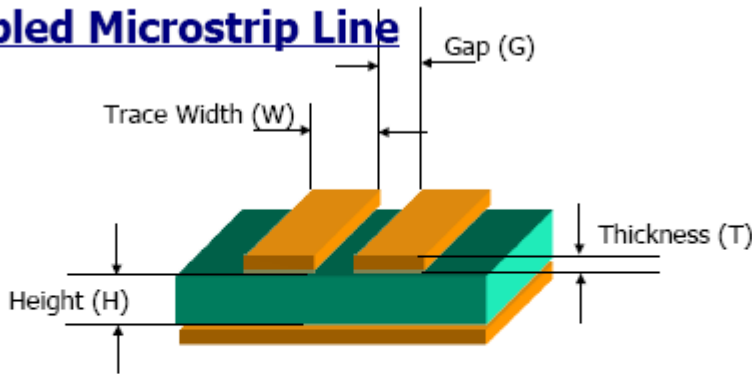


Figure 3-1 Example of APIX differential lines in a PCB Layout – courtesy of Inova Semiconductors

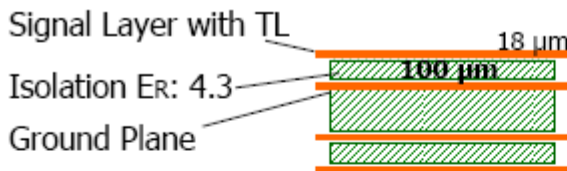
Regarding the routing of differential pairs, please see figure 3-2 for more details.

• **Coupled Microstrip Line**



- Ideal for single layer routing
- No vias required with SMD components
- 2 layer design

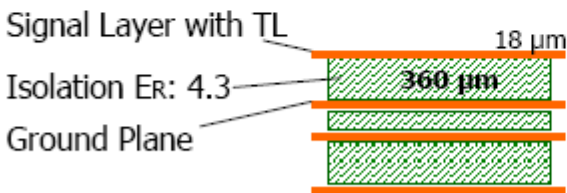
• **Examples:**



Given: $H = 100 \mu\text{m}$, $T = 18 \mu\text{m}$
Assumed effective $\epsilon_r = 3.8$

With: $W = 150 \mu\text{m}$
 $G = 120 \mu\text{m}$

$Z_{\text{DIFF}} = 2 * Z_{\text{ODD}} = 101.1 \text{ Ohm}$
Loss = 12.01 dB/m



Given: $H = 360 \mu\text{m}$, $T = 18 \mu\text{m}$
Assumed effective $\epsilon_r = 3.8$

With: $W = 360 \mu\text{m}$
 $G = 120 \mu\text{m}$

$Z_{\text{DIFF}} = 2 * Z_{\text{ODD}} = 100.7 \text{ Ohm}$
Loss = 7.08 dB/m

Figure 3-2 Coupled lines and PCB characteristics – courtesy of Inova Semiconductors

4 Components

4.1 Cable

The APIX cable should have the characteristics like a STP Cat6 cable or better. Maximum cable attenuation is:

- APIX Rx input sensitivity: 65mV
- APIX Tx drive current: 5mA at 100 Ohm : 500mV
- Max. attenuation (at 500 MHz): -17,7 dB

For more information about cable selection, please also contact [Inova Semiconductors](#).

4.2 Connector

Please use a connector with a 3dB bandwidth of minimum 1.5 GHz (e.g. [Rosenberger](#), Hirose, JAE, Honda or Molex).

Shield signal pairs in the connector from other signals.

Connect shield to ApixGND via a DC blocking capacitor. Add a bleed resistor to prevent static build up.

4.3 Parts

For a common mode choke, you can use e.g. [Murata](#) DLW21SR670HQ2 or similar.

For ESD protection e.g. SRV05-04 ([Semtech](#)) or similar could be used. Please protect to GND and 1.8V (due to lower ESD impedance GND and 1.8V are preferred to ApixGND and VDDA).

For all caps X7R is sufficient.

5 Power Supply

MB88F332 APIX requires a clean supply. Therefore the supply should be filtered with as shown in figure 3-3. Switched mode power supplies can generate spikes at very low source impedance. These are difficult to filter using only capacitors. A series inductor is therefore recommended as shown.

VDDA should be fed from the 1.8V VDD used for the MB88F332 core.

The 1.8V VDD for the MB88F332 core should be sourced from a clean supply. A switched mode power supply should be filtered with a series inductor. Note that a suitable ESD clamp may be required to ensure a low resistance path for ESD.

6 Appendix

Inova Semiconductors:

<http://www.inova-semiconductors.com/>